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ARPA IPTO

~~EXPERIMENTAL~~ PACKET RADIO SYSTEM

~~PATENT~~ ~~DESIGN PLAN~~

Repeater

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1. Parameter & Test early

2. State Military Problem

nets authentication

Comm. Exp. Spec. Sum.

3. Background on BMDS etc.

4. Definitions who sees what rep → hosts term-name overlap

5. Channel data

6. Modulation Schemes

Comp Flex 4/no

7 To spread or not-to spread

8 Channel Access

EXPERIMENTAL PACKET RADIO SYSTEM DESIGN PLAN

13 March 1974

Prepared for

Advanced Research Projects Agency
Information Processing Techniques
Arlington, Virginia 22209

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Summary

This document presents a plan for the design of an experimental Packet Radio (PR) System and provides a frame of reference for the Packet Radio Project. Within this framework, a system will be designed, experimental equipments defined, and performance measured and compared to established objectives.

Three primary goals are established for the Packet Radio Project:

a. Develop and implement a physical model of a packet switched radio network. The network is to provide the coupling mechanisms between a distributed community of interactive data terminals.

b. Investigate, develop, and demonstrate access and signaling techniques that will facilitate the application of new, technically sound frequency allocation and management strategies with the DOD.

c. Provide a research vehicle, physical model, and design data that will facilitate and support the investigations and experiments necessary to satisfy the overall goals of the integrated C3 program.

These project goals, supported by the system performance and experimental objectives, define the target for this research effort.

A packet radio system is a broadcast data network aimed at providing a local collection and distribution service for interactive data users distributed over a large geographical area. The system will be designed to be economical, reliable, secure, and responsive. There are three basic functional components of a packet radio system; the packet radio terminal, repeater, and station. A family of terminal types are covered, including personal digital terminal, tty-like devices, unattended sensors, display devices, and small computers.

The packet radio station directs the network and traffic management operations of the system and performs the accounting, directory, and route determination functions for the radio network. The station also functions as a gateway between the radio system and other packet switched networks.

The purpose of the repeater is to extend the effective range of the terminals and stations, especially in remote areas having low traffic. This increases the average ratio of terminals to stations.

The project activities up to this point have been concentrated on developing an understanding and appreciation of the problem. The project goals have been examined, clarified and refined, technical issues have been identified and structured and technical data searched out and collected. During this period, candidate approaches have been formulated and analyzed with respect to potential benefits, risks, and limitations. A

number of promising techniques have been identified and investigated, analysis tools and models have been developed and the constraints imposed on the design by the available technology have been identified and bounded. A considerable data base has been accumulated in the form of Temporary Notes and Technical Reports, some of which form the appendix section of this plan.

These investigations set the stage for a transition from investigative tasks to a concentrated design and experimentation effort. This plan identifies a point of departure and a roadmap for the development effort as well as truth points and criteria for evaluating and controlling progress toward the established goals.

In particular, this system design plan addresses the following topics:

a. System Concept. The plan identifies a concept for the design and development of a Packet Radio System. System performance objectives are presented along with primary assumptions covering application and environmental conditions. Objectives and strategies for planning and executing the project are described.

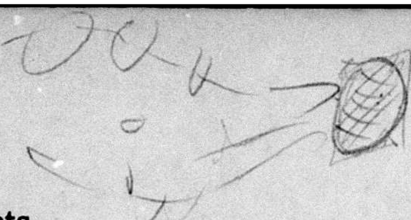
b. Initial System Design. The plan identifies and describes the design framework for the initial system implementation. A network architecture and organization are introduced along with the identification of specific design parameters (packet format, data rates, modulation type, spread factor, etc.) for the initial system configuration.

c. Prototype Equipments. The plan contains a description of a prototype packet radio repeater, terminal and station. Rf signal processing and digital functions are described along with size, weight and power estimates, and projections of performance parameters.

d. Measurement and Test. The plan introduces the objectives, strategy, and requirements for a series of experiments to check the design process. Plans for measurement and test actions are presented covering the communications link, system parameters, and various levels of network operation and performance.

This plan is a snapshot of the Packet Radio Project taken in March 1974. It shows what is to be accomplished, where we stand today, the approach being taken now, along with a plan for tomorrow. As the project progresses and the packet radio system design matures, other snapshots will be taken and the design plan reissued.

EXPERIMENTAL PACKET RADIO SYSTEM DESIGN PLAN
(OUTLINE)



Objectives

> Background = speech
> Needs of Problems
> How Modeled
> Questions -
> Signal Powers
> Issues -

> Specific Design
> Equipment Con
> Failure Conditions
> Testing Config
> .Cable
> .Remote Stn

Page

Section 1

Foreword

This document presents a plan for the design of an experimental, packet switched, distributed radio network. The plan provides a frame of reference for the packet radio project. Within this framework, a system design will be developed, experimental equipments defined, and performance will be measured and compared to established objectives.

The material in section 2 provides an introduction to the packet radio project. Goals and objectives are reviewed, approach and status are discussed, and the implementation strategy is outlined.

Section 3 addresses the subject of coexistence. The many dimensions of the problem are identified, varying degrees of coexistence are introduced, possible technical approaches are introduced, and a plan of attack on this complex question is outlined.

Performance objectives and constraints are introduced and discussed in section 4. This section provides the benchmark against which the accomplishments of the design process will be measured.

The initial system design is presented and discussed in the next two sections. The network architecture is described and network elements identified in section 5 and such system characteristics as routing procedures, flow control, and packet format are detailed.

The initial rf system design is described in section 6. Link and channel parameters are defined, and access schemes are identified. Promising alternative designs for the rf system are introduced.

The measurement and test program is presented in section 7. The experiments discussed in this area are designed to measure the design and the project performance against the established goals and objectives.

A plan for the design of prototype equipments to implement the initial system design is contained in section 8. A family of functional elements is identified and discussed and the characteristic of a prototype repeater, terminal, and station are projected.

The design plan previewed above is one result of an investigation and definition effort directed at all facets of the radio network question. The appendix to this plan contains reference material generated during this investigation phase. This material contains the rationale for the initial system design and extends the level of technical detail in many areas.

It is important to emphasize that this design plan is not a specification or a final report, but a working document. It represents a snapshot of the project taken at a particular point in time. The system and equipment designs presented will change as new ideas are generated and/or test results do not come up to expectations. The net result is that the plan will be revised and reissued on a non-periodic basis, with the time between revisions governed by the results of the design process.

The design plan is only one of three types of documents associated with this project. Companion documents are implementation plans and notes and reports directed at specific technical issues. The implementation documents translate the direction and strategy statements of the design plan into specific task and schedule-oriented descriptions that are necessary for the day-to-day management and coordination of the project activities.

Section 2

Introduction to Packet Radio: The Program, Goals and Objectives

2.1 BACKGROUND

In 1968, after considerable research and investigation, the Advanced Research Projects Agency (ARPA) embarked on an experimental project to create a nationwide computer resource-sharing network. The primary goal of this project was to permit persons and programs at one research center to interactively access and use data, programs, and computing resources that existed at other research centers.

how many more?

This project is nearing completion; a network of more than 40 nodes exists today with a measured performance that exceeds the original project goals. The success of the ARPANET has served to focus attention on the many promising applications for this technology, and at the same time has emphasized deficiencies and the need for new techniques and tools in related areas. Two observations that emerged from a review of the ARPANET applications and technology were:

a. The full potential of resource-sharing networks would not be realized until new techniques were uncovered that provide a high quality, flexible, responsive terminal access capability.

b. The tremendous advances in digital processing technology made packet switching a very promising candidate for this interactive data communication application.

In the early 1970's, ARPA initiated research investigations directed at extending the packet switching technology into the area of rf communications. The ALOHA project investigated and implemented an experimental packet communication net based on radio broadcast properties. The ARPA Satellite Project is presently implementing a packet switched satellite-based system. This application utilizes the unique broadcast properties of satellites coupled with the burst character of packet organized traffic to provide a high capacity distributed switching mechanism with large area coverage.

These projects – the ARPANET, ALOHA, and Packet Satellite – set the stage for the definition of the packet radio effort. A number of the tools and disciplines needed to achieve a global interactive resource-sharing capability had been established, but certain voids still existed. The need for this network technology was recognized and the Packet Radio Project emerged.

2.2 PROJECT GOALS

The packet radio (PR) project is one element of an ARPA research program that is focused on integrated command, control, and communications (C^3) structures and technology.

Specific goals have been established to provide direction and checkpoints for the PR investigations. These goals were selected to allow the PR project to proceed with a minimum of dependence on the other network activities, but at the same time to ensure that the PR results are generated within the framework of the C^3 Program.

Three primary goals are recognized for the PR project: The first goal addresses the communication or packet transportation issues associated with a distributed, mobile community of interactive data terminals; the second goal is directed at the critical shortage of rf spectrum and the need for improved frequency management strategies; the third goal identifies a relationship between the PR project and the research activities planned in the integrated C^3 area.

2.2.1 Radio Network Goal

The radio network goals include the development and implementation of a physical model of a packet switched radio network. The network is to provide the coupling mechanisms between a distributed community of interactive data terminals and other resource-sharing and/or information processing networks. The network will provide packet access and distribution for a variety of terminal types including mobile/portable data terminals, minicomputers, unattended sensors and hand-held input/output devices. TTO?

The network provides a concentration function; all terminal traffic is directed at, or exists from, a station. The overall network connection pattern is a bidirectional N to 1 matrix.

The packet transportation subnet is one part of the terminal access/distribution network. The transportation subnet contains all of the rf and signal processing capability, the management disciplines and logical processes required to handle the movement of packets back and forth between terminal ports and the station. User protocols, interactive communication functions, and internetwork or gateway features are not included in the PR research goal.

Three classes of terminal applications are identified for purposes of the rf system design and evaluation.

a. Fixed Terminal. The terminal equipment will be fixed for long time periods (months to years). The antenna and rf equipment site can be selected within certain limits. Size or cost? (few)

b. Transportable Terminal. The terminal equipment is moved from place to place, but only needs to operate when stationary. The terminal can be positioned within limits (10's of feet) for best operation. Size or cost contrain (many)

c. Mobile Terminal. The terminal equipment must operate when the terminal is in motion with respect to repeaters/stations.

many

The initial test of the system will be as an access mechanism to a resource-sharing network (the ARPANET) for message and computational services.

The ultimate target for this research effort is the DOD C^3 application. The PR technology must be applicable to military tactical systems and the access/distribution functions associated with WWMCCS.

2.2.2 Frequency Management Goal

Investigate, develop and demonstrate access and signaling techniques that will facilitate the application of new, technically sound frequency allocation and management strategies with the DOD.

Provide dynamic allocation mechanisms for sharing a limited quantity of rf spectrum between a large community of user terminals. The mechanisms are to be structured such that control can be distributed throughout the network and that spectrum utilization is optimized in terms of network, not link, traffic.

Provide signaling strategies that will ensure a degree of coexistence between PR networks and other radio systems. The intent in this area is to select a frequency band that is not reserved exclusively for PR and by careful selection of parameters and signaling strategies to achieve, within certain limits or bounds, two-way coexistence between the PR network and the radio systems that presently exist in the band. The PR network must be able to accomplish its mission in the rf environment created by these other systems. Also, introducing PR network into this environment must not adversely effect the performance of other radio systems.

2.2.3 C^3 Research Goal ← Too broad - Military goals - problem?

Provide a research vehicle, physical model and data base, that will facilitate and support the investigations and experiments necessary to satisfy the overall goals of the integrated C^3 program.

The PR network, in conjunction with other research tools (ARPANET, Packet Satellite, etc.), represent the basic elements of a global, interactive digital network. This capability is a prerequisite for the investigation and transfer of such promising subjects as internetwork connection disciplines, user protocols, end-to-end encryption, distributed data base management, and management system modeling. too broad

2.3 GENERAL APPROACH

Three general phases of project activity have been identified.

- Investigation and Definition Phase
- Design and Experimentation Phase
- Evaluation and Transfer Phase

These general categories are not sharply bounded task areas, but represent the shift in the thrust and emphasis of the research effort as the project progresses.

The activities during the investigation and definition phase are concentrated on developing a true understanding and application of the problem. The project goals are examined, clarified and refined, technical issues are identified and structured, and technical data is searched out and collected. It is during this phase of the project that candidate approaches are formulated and analyzed with respect to potential benefits, risks and limitations.

The PR project is well into this initial phase. A number of promising techniques have been identified and investigated, analysis tools and models have been developed, and the constraints imposed on the design by the available technology have been identified and bounded. A considerable data base has been accumulated in the form of temporary notes and technical reports. This sets the stage for the transition to the design and experimentation phase.

In the design and experimentation phase, the emphasis is on "making it happen." This period represents the growth cycle of the project: network and system parameters are selected, control algorithms are designed and coded, the capability for testing and experiments is created, hypotheses are tested, mistakes are identified and corrected, and the many diverse parts are forged into a system.

This experimental packet radio system design plan signals the start of a concentrated design and experimentation effort for the PR project. The plan identifies a point of departure and a roadmap for the development effort as well as truth points and criteria for evaluating and controlling progress toward the established goals.

The final phase of the PR project consists of the activities required to terminate the project in an orderly, positive manner. Accomplishments are measured with respect to original goals, conclusions are drawn, judgments are made with regard to follow-on opportunities and the physical models and research data are packaged for transfer to the projects that will follow.

2.4 OBJECTIVES FOR EXPERIMENTS

A series of activities and experiments are planned that form an ordered and control process leading to the satisfaction of the established project goals. Each experiment is designed to satisfy one or more of the following criteria:

a. To prove or disprove a particular design assumption.

b. To provide data points for the validation of design aids-models and simulations.

c. To gain insight into the impact of alternative design strategies.

d. To access performance with the system elements interacting in their natural environment.

The experiments are structured to provide checkpoints and measures of accomplishment for project monitoring and control.

The following objectives have been established for the planned experiments:

a. Identify difference between predicted and actual radio link performance in such areas as: bit error rate (BER), range contours, and transfer reliability.

b. Assess the performance of a community of terminals and repeaters sharing a common rf channel. Performance measures include: number of blocked packets, capture statistics, packet error rates, and interference profiles.

c. Assess the impact on performance of alternative design approaches for: channel access and management, power level mechanisms, and routing techniques.

d. Determine the degradation in transfer performance caused by signals emanating from other rf systems in the same general area.

e. Identify specific rf systems that may be interfered with by the Packet Radio signals. Conduct cooperative experiments with the systems to identify interference relationships.

f. Measure performance parameters of an isolated PR network containing terminals, repeaters and stations. Performance measure includes: network throughput, capacity, delay, etc.

g. Access the impact on network performance of alternative design strategies in such areas as: routing, addressing, flow control, network management, initialization, recovery routines, and multiple stations.

h. Connect the radio network to the ARPANET and demonstrate the access/distribution function.

2.5 IMPLEMENTATION STRATEGY

The planned implementation sequence is designed to provide a balance between the need for a thoughtful, well-conceived design of the system and the companion need to prove or disprove the design via experiments and tests in a representative environment. To accomplish this balance, a "Packet Radio" laboratory is planned. Initially, a small laboratory is required. As the design process continues and the experimental results are evaluated, the research capacity is increased and a network laboratory evolves. where?

To control this process, five stages of experimental capacity are identified. The stages are determined such that each one provides a significant new dimension for experimentation and each requires an additional commitment of resource to provide the research vehicle.

The experimental elements required at each stage along with an identification of the experimental objectives addressed in each case are outlined in the following paragraphs: in the military where?

a. The first stage is concerned with the characterization of the rf environment. The research capacity needed is the propagation/noise test system. The experiments planned at this level are designed to establish and refine the propagation models and model parameters. This capability has been implemented and the planned measurements are underway.

b. The next level of planned implementation consists of three rf elements and associated processing and input/output (I/O) devices. The three elements can be configured to perform as packet generators or repeaters. With this level of research capacity, experiments will be conducted that address objectives a. through e. of paragraph 2.4.

c. The third stage is reached when one station and 13 rf elements are available in the experimental system. At this level, we have a powerful physical model that is suited for a wide range of network experiments. Network performance will be measured and promising alternatives investigated.

this just generates the system does not test it

d. The transition to the fourth stage is achieved by adding a second station to the network and interconnecting one of the stations as an ARPANET gateway. This allows experiments in such areas as multiple station operation, initialization procedures, handover, and recovery routines. It also allows access to the ARPANET resources for such services as data collection and traffic generation.

e. The final configuration defined consists of two stations, both configured as gateways, and 25 rf elements. The additional rf elements are configured as terminals to facilitate a community of users to access the ARPANET via the packet radio network.

The activity and progress between implementation stages is not represented by a smooth curve or a series of step functions. Rather, it must be viewed as having an irregular shape. The situation at any particular point in time is determined by the experimental results. If a high confidence is indicated, additional equipments may be introduced to facilitate the evolution toward the next stage or checkpoint. Discouraging results might require modification of the experimental equipments and the design and execution of additional tests.

3.1 BACKGROUND

The ability of today's radio systems to operate with some measure of protection from rf interference is primarily achieved through policy, regulation, and allocation procedures. The rf spectrum is organized into bands in accordance with broad classes of service defined by the International Telecommunications Union. Governing bodies have been established, both national and international, to set policy, control and monitor the use of rf resources. Each of these governing bodies has rules and specifications covering the type and characteristics of rf systems that can be permitted to operate in particular segments of the spectrum and/or geographic areas.

These rules and specifications divide an rf band into a finite number of discrete blocks and provide frequency and/or distance guard bands that ensure isolation between systems. Licenses for a system to operate, in a particular frequency block at a particular location, remove that portion of the rf spectrum from the resource pool for extended periods of time (years to decades).

This static allocation mechanism, the fact that only a finite amount of spectrum is available, and the rapidly increasing demand for spectrum resources, have produced an "rf spectrum crises." One of the primary goals of the packet radio project is to find rf signaling and channel management strategies that will provide relief in this area.

3.2 A GENERAL COEXISTENCE MODEL

Coexistence is a two-edged sword. One edge deals with inserting a radio system into an area and the rf environment existing in that area, and ensuring that the performance of the existing systems is not degraded below tolerable bounds. The other edge is that the new system must be able to perform its intended mission while emersed in the rf environment created by the existing systems. The question then, translated to the research vehicle of the packet radio system, is "What is the effect on the performance of neighboring radio systems when a packet radio (PR) network, is introduced into an area ?," and "What performance can we expect from a packet radio network when we introduce it into a particular rf environment?"

3.2.1 Basic Model Structure

The basic structure of a coexistence model consists of a receiver or sensor emersed in an electromagnetic field. A portion of the energy associated with this field is the desired signal from a companion radiating source or sources, and the remaining energy is interference. The interference can be related to natural causes, manmade (but not radio system) sources, and other rf systems operating in the same band and propagation area.

Figure 3-1 illustrates the basic degrees of freedom of the generalized interference model. A sensor is shown along with a companion radiating device. The path labeled D_0 represents the data transfer link associated with the assigned mission of the system. A community of other radiating sources is shown, each of which are external to the system envelope of the subject sensor or receiver.

The sensor could be a repeater receiver and the one radiating element another PR equipment if the focus of the model were the impact on a PR network of external systems. If working the reverse part of the question, the sensor would represent the receiving site in question and the interference sources would be PR network elements.

The focal point of a meaningful analysis is the performance of the receive detector when subjected to the composite energy of the multiple signals impinging on the antenna. To determine the detector performance requires knowledge of the sensor characteristics (from antenna to detector), the characteristic of each source element, and the geographic factors (distance, elevation, obstructions, etc.) relating each source to the subject receiver.

3.2.2 Model Parameters

As indicated in the preceding paragraphs, a knowledge of the characteristics of each element in the model is required. The primary parameters needed to provide such a characterization are outlined in the following paragraphs.

Sources must be characterized in terms of the distribution of energy radiated from the antenna as a function of frequency, time, and space or direction. The parameters of interest include:

a. Peak power

b. Antenna gain

c. Directivity — mainlobes and sidelobes

d. Power spectral density

e. Duty cycle

f. Center frequency.

At the sensor one is interested in the energy transfer function between the antenna and the detector. Parameters of interest for receivers include:

a. Antenna capture area

b. Antenna directivity

c. RF bandwidth — frequency and phase response

d. Receiver sensitivity

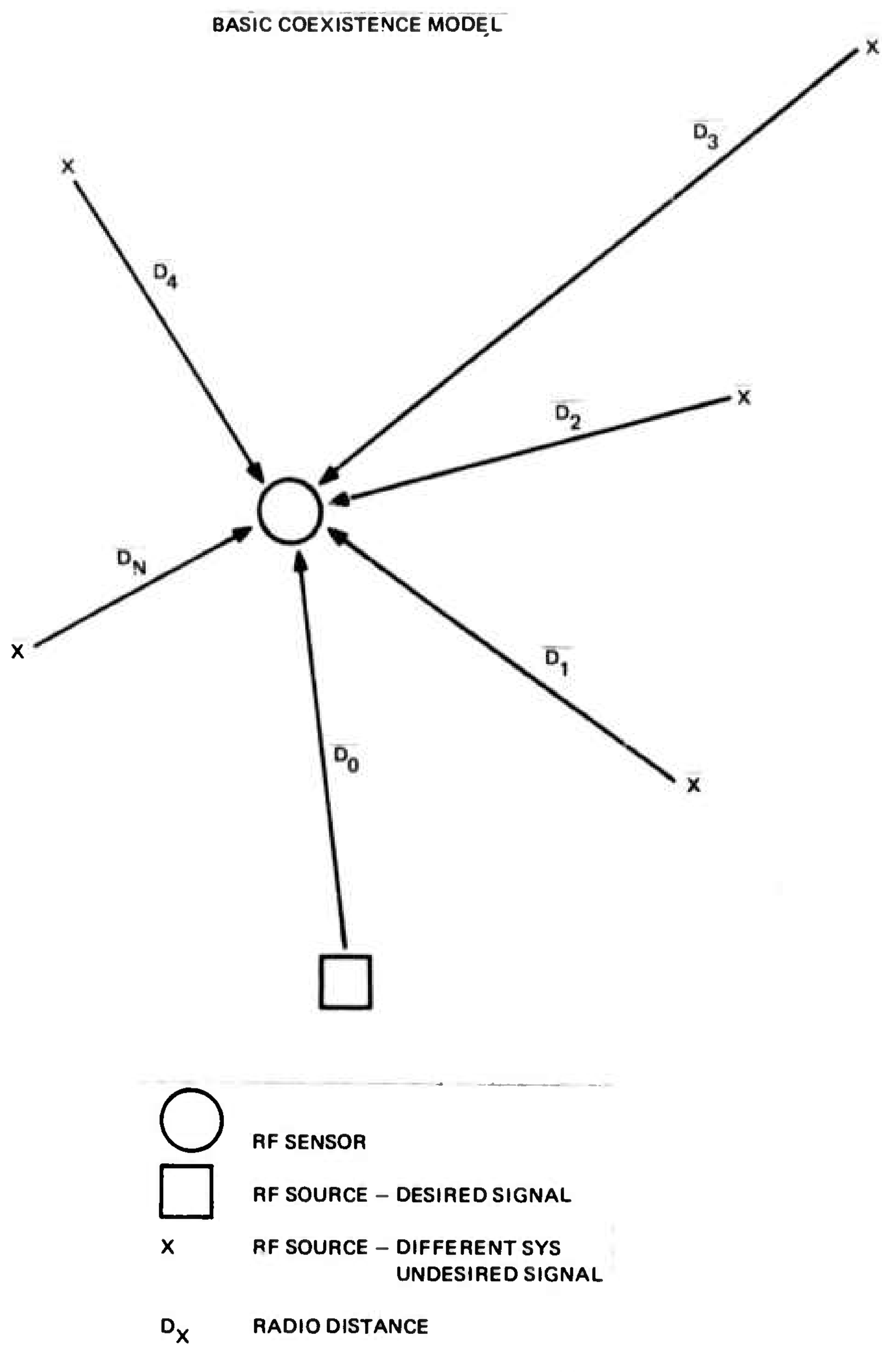


Figure 3-1. Basic Coexistence Model.

e. Dynamic range

f. Processing gain

g. Detector transfer function.

The common factor between source and sensor is the distribution of rf energy. To translate between the energy radiated at a source and the energy impinging on the receive antenna, geometry and the nature of the propagation path must be introduced. Pertinent parameters for this include:

a. Range

b. Direction

c. Relative elevation

d. Path losses.

deliberate jamming

In the design of the packet radio system, the source and sensor characteristics of the PR system elements will be defined. Values must be established for these parameters such that the basic data transfer mission of the network is satisfied and within the additional constraint that the mutual interference (between the PR network and other rf systems in the selected frequency band and geographic areas) be within tolerance.

3.3 BASIC APPROACHES

The subject of coexistence has been shown to have many dimensions and degrees of freedom. In organizing possible approaches to this complex problem, one can consider degrees of coexistence. It is extremely difficult to conceive of a solution, or for that matter even a way to start, that would ensure coexistence between all systems, under all conditions, with no limits or exceptions. It is possible to consider sub-sets of the question that will provide for coexistence over a usable range of conditions and system parameters.

One possible sub-set of the coexistence question is that of directly sharing a frequency sub-band with another system. In this case, the packet radio system would be directly overlayed on an operating frequency domain allocated to a different type of service and equipment. One can conceive of doing this in any one of several existing bands, but the PR system design could be different for each specific case. A simple example of this approach would be a frequency band presently occupied and specified for satellite up-link service. PR system could be designed to share these frequencies directly on a non-interfering basis.

Another promising prospective on this question is to achieve coexistence by designing the PR system to utilize those portions of the spectrum presently required for guardbands or isolation between existing systems. Several options are possible when this degree of freedom is explored.

a. Geographic Isolation. One dimension of today's allocation procedure is to ensure geographic separation between radio systems that occupy the same frequency. For

example, if uhf tv Channel 39 is licensed in Dallas, Texas, the same channel will not be allocated to any station within a prescribed radius of the Dallas area. It is possible to design a PR system with the rf signature tailored such that it could be installed and operated to provide service to an area located midway between two such uhf tv stations.

b. Frequency Separation. Today's allocations provide guardbands between individual frequency channels established with a band. A PR system could be designed that would use one or more of these narrow frequency windows to support the data transfer requirements of the network.

Regardless of the degree of coexistence to be considered, methods and techniques of tailoring the PR system rf signature to the target environment and providing a degree of immunity for a PR detector from the ambient rf are required. Candidate approaches in this area provide a second level of design freedom.

a. Spread Spectrum Techniques. Application of these techniques provides a reduction (from the nonspread case) of the transmitted power density and provides processing gain at the receiver. FFH ?

b. Error Correction Coding. A robust receiving system can be defined through the use of error correction coding to provide additional immunity to interference.

c. Selective Filtering. The rf signature and/or the receive transfer function can be tailored to meet a particular set of conditions. Several techniques can be used to implement this technique, including discrete filters, cancellation mechanisms, and digital processing.

3.4 PLAN FOR THE EXPERIMENTAL SYSTEM

The question of coexistence is complex and a number of different approaches are possible. The highlights of the plan under which the project is now proceeding are presented in the following paragraphs. The primary objective is to establish coexistence in a particular operating frequency band.

a. Select a Target Band. A portion of the spectrum will be selected for the PR system design. This band will be occupied by existing radio systems. The effort to date indicates that the 1710- to 1850-MHz band is a good choice, that is, it meets the PR needs and has a sufficient number of existing system users for a meaningful coexistence experiment. No!! why? No!

b. Develop Criteria and Measures. This effort is presently underway and consists of a more precise definition of the problem. The criteria with which we can evaluate specific technical options and the measures corresponding to these criteria must be sharply defined.

c. Characterize Existing Systems. A detailed knowledge of the characteristics of the systems with which we desire to coexist is required. For the target band selected, each system type will be characterized in terms of source parameters, sensor parameters, and geographic factors.

d. Overlay and Evaluation. The characteristics of the initial PR system design will be overlayed on the characteristics defined per item c. above. A degree of isolation will be projected and specific experiments planned. Also, selected alternative design will be overlayed and evaluated using the same criteria and measures. The results of this comparison, coupled with experimental data, will be used to rank the initial system design.

e. Experiment and Verify. The initial system design, and possibly other promising alternatives, will be tested in the selected band under operational conditions to prove, disprove, or modify the coexistence estimates.

f. Coexistence Guidelines The results of the research and experimentation will be used to develop a generalized theorem of coexistence. The impact of this theorem on present policy, practices, and procedures will be identified.

Section 4

Objectives and Constraints

4.1 GENERAL

The following objectives and constraints have been established by preliminary synthesis of the desirable properties of an experimental system. These will be modified as potential applications indicate new or changed requirements and as experience with the experimental system indicates modification is needed or possible.

4.2 OPERATIONAL PERFORMANCE OBJECTIVES

Although the initial network will be designed to support a variety of measurements and experiments, the long range objectives of the packet radio project include the ultimate transfer of packet radio (PR) technology to military users. Thus, the experimental network must be developed and the measurements and experiments must be accomplished with a set of operational objectives in mind. The experimental network will either meet these objectives or demonstrate the feasibility of meeting these objectives with a simple extension of the technology used.

4.2.1 Bit Rate

The experimental network will be supported by the terminal-repeater (TR) and the repeater-repeater (RR) links.

The TR channel bit rate is an important parameter since it determines peak data transfer rate, as well as the number of fixed-rate users per channel. The physical limitations of the channel, including multipath propagation and noise, are such that bit rates up to perhaps 500 kBps are possible with complex anti-multipath schemes; however, such data rates require high peak power in the terminal to achieve reasonable range. A target bit rate of 100 kBps has been selected for the TR link since it would provide a significant improvement over existing mobile communications data rates and would meet most immediate military needs. This target bit rate will be possible to achieve with state-of-the-art hardware.

A bit rate of 500 kBps has been chosen for the RR link since the repeaters are expected to be placed above the surrounding terrain and will experience less propagation loss (and less multipath) when operating RR than when operating TR.

4.2.2 Delay

The network delay is specified as the delay experienced by a user in transmitting a packet from his terminal to the station and receiving a response. The time that the station requires to compute or otherwise generate a response is not included. Ideally, a transparent network would add no delay; however, network throughput and delay are inversely correlated so that such a network is impossible. Long delay times in interactive data systems discourage users and may be intolerable to military users; however, short delays are possible only if the channel is not heavily loaded. The design goal for average end-to-end delay has been set as 0.1 second.

4.2.3 Error Rates

Several types of errors are possible in a PR network. For example, a packet may be "lost," or it may be transmitted with textual errors. The sum of these errors from all causes should be highly improbable in the packet radio network. A goal is to limit uncorrected errors from all sources to 1 error in 10^{12} packets.

4.2.4 Security

To be useful to the military, a PR network must be capable of operation in a secure mode, and the experimental network must be designed so that such capability is demonstrable. Security, like other performance parameters, is not an absolute. It must be specified in terms of the probability that a threat of specific sophistication will accomplish an anti-system act in a fixed period of time. Such specification is usually reserved for communication systems designed to meet specific operational tasks. This system, as an experimental network, will be designed with security in mind but will not meet threat-specific requirements. System design will incorporate anti-spoof and low-detectability features. Provision will be made for end-end encryption, and the key-distribution problem will be solved. ?

How about deliberate saturation?
or insertion of spoofing packets

4.2.5 Uniformity

Because of the geographical distribution of the users of a PR network, it is possible that all users do not experience equal performance. A design goal will be to provide uniform error rates and delay throughout the PR network.

Not Rational
Could be variable and probably should

4.2.6 Transparency

The PR network must support a wide variety of mobile and fixed users. To be useful, it is important that the user find the network transparent. A hand-off form repeater to repeater should be automatic and require no user interaction. All network communications functions should be transparent to the user so that he experiences only a slight delay. That is, he should not be required to point antennas, tune receivers or transmitters, acknowledge messages, etc. All necessary protocol should be accomplished automatically by the terminal and repeater.

4.2.7 Maintenance Cycle

The repeaters should be designed to operate unattended for long periods of time. All maintenance, including battery replacement should require only one repeater-site visit per week.

The terminals should meet the same requirements; however, daily battery replacement is acceptable.

4.2.8 Network Relocation and Expansion

A primary military use of such networks would involve a requirement to rapidly relocate, extend, or otherwise modify the coverage of a PR network. The experimental network will be designed in such a way that this capability can be demonstrated.

4.2.9 Modularity

For economic and logistic reasons it is desirable that the PR network be developed in a modular fashion. All components (repeaters, stations, and terminals) should be built out of a set of a few standard modules.

4.3 USER CONSTRAINTS

One goal of the PR project is to examine the communication issues associated with a distributed community of mobile interactive users. This goal places some user-oriented constraints on system design.

4.3.1 Mobile Terminals

The network must be capable of supporting mobile users moving through the network at speeds up to 100 mph. not a/c ?

4.3.2 Portable Repeaters

The objective of rapid and easy mobility places size and weight constraints on the repeaters. The repeaters, excluding power source, will not exceed 45 pounds or 1 cubic foot as a design goal.

4.3.3 Terminal Variety

The network design will be capable of supporting a variety of terminals including, as a minimum, teletype-speed printers and displays, high-speed line printers and displays, and minicomputers.

4.4 OPERATING ENVIRONMENT

The criteria used in choosing the geographical area for the experimental network were for the area to have a wide variety of operational environments in which the network must certainly operate and for the area to approximate the more severe military environments in which the network must ultimately operate.

4.4.1 Propagation Constraints

The network will operate in the multipath environment typical of a worst-case topology such as an urban high-rise area or a jungle. In such an environment no degradation in performance should be experienced; however, decreased repeater coverage may be necessitated and is acceptable.

4.4.2 Noise Constraints

The network will operate in a typical urban noise environment where manmade noise predominates.

4.4.3 Coexistence

In the military context, it is important that the network be capable of operation in a military rf environment. The experimental network should demonstrate an ability to operate in typical military rf interference, and it should demonstrate that it does not interfere with friendly systems. This rfi objective implies more than the usual rfi specification. A major goal of the program is to demonstrate new and more efficient ways to use the spectrum. Coexistence is a primary requirement in this demonstration.

4.5 ECONOMIC OBJECTIVES

The ultimate realization of the packet radio system must be economically competitive or superior to other applicable methods of data communication. Hence, cost performance comparisons (with other viable communication options) must be established. This implies that common measures of performance for packet radio and its alternatives must be derived to allow meaningful comparison.

Among the alternatives to be considered are multidropped shared communications lines, looped communications systems, and two-way coaxial cable systems. Measures reflecting the cost throughput, delay, and reliability characteristics of these systems will be identified. Packet radio system tradeoffs such as components cost, repeater and station area coverages, and a number of simultaneous users of the system will be derived. This data will be used to derive large quantity cost and performance requirements for the packet radio system elements.

4.6 REQUIREMENTS TO SUPPORT EXPERIMENTS

A major goal of the experimental network will be to support experiments and measurements designed to explore packet communication issues. Section 7 is devoted to these objectives. Briefly, the network must have built-in capabilities to measure network delay and traffic statistics. The components must be designed so that experiments with alternative system or subsystem designs are possible.

5.1 INTRODUCTION

The packet radio system is a broadcast data network aimed at providing local collection and distribution of data over large geographical areas. The system is designed to be economical, reliable, secure, and conservative of spectrum. There are three basic functional components of the packet radio system: The packet radio terminal, the packet radio station, and the packet radio repeater. (See figure 5-1.) Packet radio terminals will be of various types, including personal digital terminals, tty-like devices, unattended sensors, small computers, display printers, and position location devices.

The packet radio station is the interface component between the broadcast system and point-to-point network. In addition, it will perform accounting, buffering, directory, and routing functions for the overall system.

The basic function of the packet radio repeater is to extend the effective range of the terminals and the stations, especially in remote areas of low traffic, and thereby increase the average ratio of terminals to stations.

The devices (repeaters, stations, and terminals) of the packet radio system communicate in a broadcast mode using a random access method suitable for:

a. Terminals that are mobile, so that a broadcasting mode is necessary

b. Terminals that are located in remote or hostile locations where hardwire connections are not feasible

c. Terminals that have a high ratio of peak bandwidth to average bandwidth requirements (because the random access method allows the dynamic allocation of channel capacity without centralized control)

d. Terminals that require little communication bandwidth so that hardwire connections are uneconomical.

Stations will be allocated on the basis of traffic. In regions of low traffic density, the station may not be in the line-of-sight of all the terminals in the region; hence, repeaters are used to relay the traffic to the station. Thus, repeaters correspond to geographical partition of the area into sections small enough so that each terminal can communicate with a repeater and be relayed by it to a station.

In areas of high traffic, such as urban areas, repeaters may not be needed; in fact, the problem may be that a station can communicate with more terminals than it can handle.

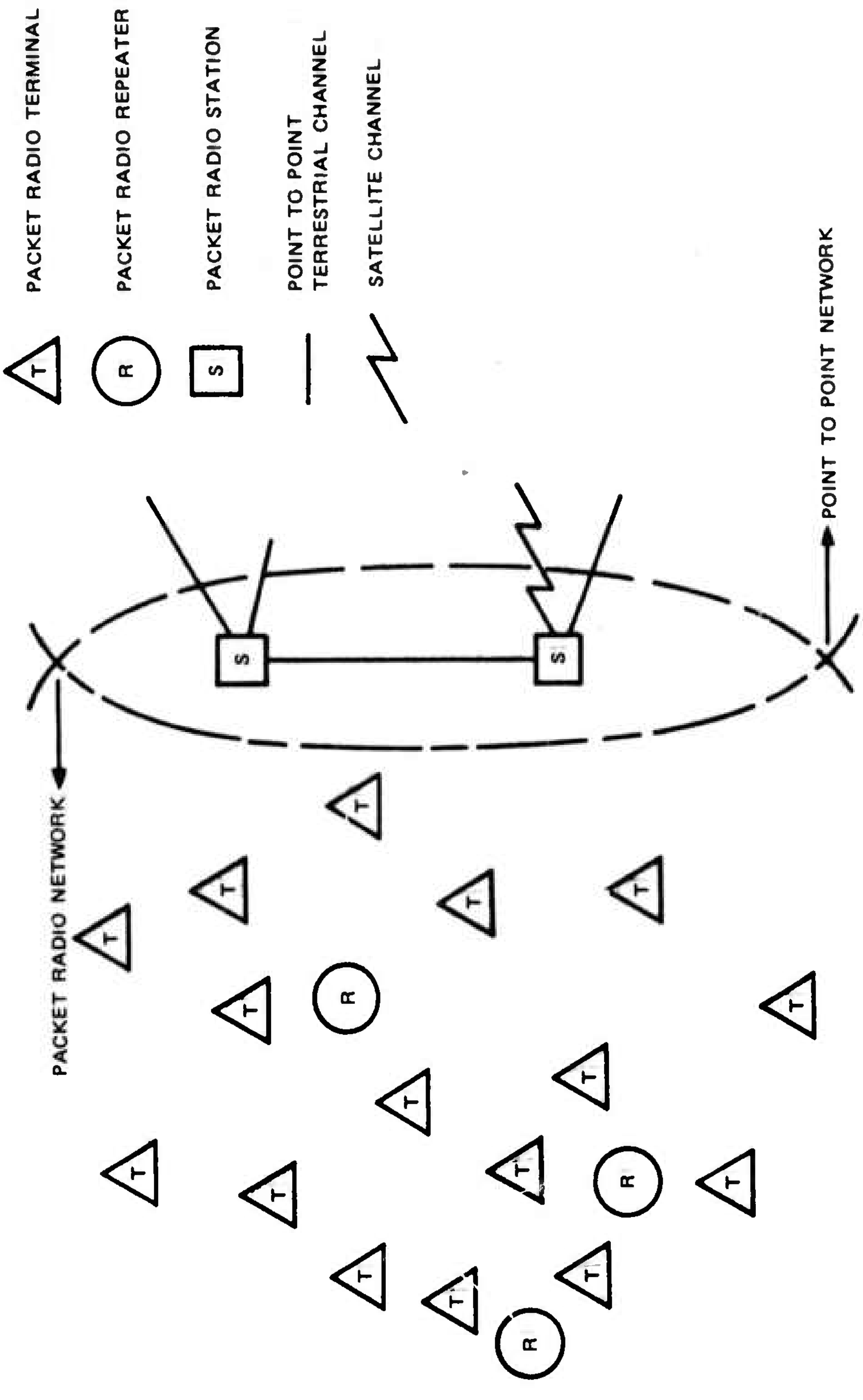


Figure 5-1. Packet Radio System.

Broadcast of data in urban areas is also complicated by extreme multipath interference. The rapidly expanding cable television (CATV) systems within urban areas offer an attractive alternative to over-the-air broadcasting, except for mobile users who must use broadcast techniques. The same general packet radio concept can be applied to packet communication on coaxial cable systems.

In this section we outline the various algorithms and procedures to be tested in the experimental system and the requirements that these imply on the design of this system.

Emphasis is placed on testing procedures related to the overall system performance rather than to the detailed performance of particular devices; that is, system protocols, throughput, delay, loss, routing, management and control, reliability, and the major parameters which affect these are discussed. The procedures to be tested that are outlined in this chapter are implemented primarily through software features (rather than hardware). Some of the requirements outlined may not be implemented in the first experimental system, e.g., some of the multistation experiments. These will be tested by simulation and possibly by the experimental system at a later date.

5.2 GENERAL SYSTEM CONFIGURATION

5.2.1 Network Topology

The following factors affect the topological design of the packet radio network (PRNET):

a. Capacity considerations, e.g., the number of stations needed

b. Area coverage, including topographical considerations

c. Logistics, such as device accessibility and power availability

d. Reliability and redundancy, e.g., a requirement that any possible terminal location should be able to communicate with at least two repeaters, and a similar connectivity requirement in the repeater-station network

e. The routing and flow control used that affects the traffic patterns and, consequently, impacts on the topological design

f. Special design considerations, such as the critical hop, the power duty cycle of devices, and others.

The first experimental system may not be sufficient for studying all the factors that affect the topological design. However, many general topological characteristics can be simulated, such as low and high intereference topologies and networks on different topographical areas. The only requirement that the above experiments place on the devices is that they be easily accessible and be easily movable from one location to another.

5.2.2 Communication Channels

Two data signaling rates (nominally 100 kBps and 500 kBps) should be provided to repeater and station, and one data rate (1000 bits/s) to the terminal. The high data rate will be used for signaling in the repeater-station network, and the low data rate for signaling between terminal and repeater or terminal and station. There should be a possibility of using the low data rate in the repeater-station network. The channels should operate in a half duplex mode. This will enable testing of the channel configurations that have been studied theoretically in detail. Among these configuration are: Common Channel Single Data Rate (CCSDR), and Common Channel Two Data Rates (CCTDR). Repeaters should have the capability of receiving a packet at one data rate and repeating it at another data rate.

5.2.3 Access Modes

Two possible access modes should be provided to all devices: the non-slotted Aloha mode and the Carrier-Sense mode. The particular carrier-sense protocol of interest is the nonpersistent carrier-sense. This protocol is defined as follows: When a packet is ready for transmission, the device senses the channel; if the channel is idle, the device transmits the whole packet, otherwise the packet is scheduled for some future random time at which the channel is sensed again and the procedure repeated.

The interval of time over which the rescheduling time is distributed (presumably uniformly) and the interval of time during which the channel is sensed should be software implemented. To compare with simulation results, one would have to implement the smallest possible sensing time sufficient to determine the presence of an rf signal. Note that by implementing a sensing time below the threshold needed to detect the presence of an rf signal in the nonpersistent carrier-sense, one automatically obtains the nonslotted Aloha random access mode. Parameters for the access modes will be transmitted to repeaters from the station and modified. This can be used by the station to control the traffic flow on critical hops.

5.2.4 Adaptive Power

All devices, in particular the repeater and station, should be provided with several (at least three) power levels. The power levels should be software selectable.

a. The use of adaptive power should enable the terminal to identify the repeater (station) nearest to it, thus reducing the interference level and preserving terminal power.

b. The adaptive power control at the repeater can be provided either by a repeater algorithm (e.g., as a function of the number of transmissions before success), by control packets from the station, or by both.

c. In addition to monitoring the interference level and preserving power, adaptive power will be investigated as a means to enhance network reliability. For example, when several repeaters in the network are down, the station can instruct a set of repeaters (or all) to operate at high power.

d. The station can use the adaptive power to control the number of repeaters and terminals that it can reach. For example, when transmitting an information packet to a remote terminal, the station may use the maximum power to reach a remote repeater or possibly the terminal. In this case, the station may give up the possibility of receiving an hop-by-hop acknowledgment (HBH Ack) and wait only for the end-to-end acknowledgment (ETE Ack).

5.2.5 Antennas

Station, repeater, and terminal should be provided with omnidirectional antennas. The station should also be provided with the ability to attach directional antennas.

5.3 ROUTING ALGORITHMS

Three routing algorithms are briefly described in the following paragraphs. These and their variations are recommended for implementation and testing in the experimental system.

5.3.1 Hierarchical Labeling

The hierarchical labeling routing scheme enables point-to-point routing between devices along an "efficient path." It is obtained by assigning to every repeater a label, which forms, functionally, a hierarchical structure. The label assigned contains the following information:

a. A specific address of the repeater for routing purposes

b. The minimum number of hops to the nearest station

c. The specific address of all repeaters on the shortest path to the station, and the address of the repeater to which a packet has to be transmitted when destined to the station.

In the hierarchical labeling algorithm an information packet (IP) is addressed to one device. If it is received by a device to which it is not addressed, then the receiving device is closer to the destination than the device to which the packet was addressed. If the preassigned path is temporarily blocked, the packet may depart from it. It then uses the most efficient path from its new location.

5.3.2 Directed Routing (One Level Labels)

Directed routing is a simplified version of the hierarchical labeling algorithm in which the only information preserved is the direction TO or FROM station. Repeaters are assigned labels that indicate the hierarchy level, or the number of hops to the nearest station. When a device transmits a packet, the packet is addressed to all repeaters (stations) that are closer to the destination than the transmitting device. Many devices can receive the same packet and it may arrive at more than one station. The acknowledgment schemes, the station-station protocol, and the station-terminal protocol must then resolve this problem.

5.3.3 Undirected Routing Plus Repeater Memory

In this algorithm there is no directionality of transmission. A packet is addressed to all devices that can hear it. To control the problems of cycling and looping, repeaters are assigned storage for unique identifiers of packets that they recently repeated. When a packet is received by a repeater, it compares its identifier with those stored and discards the packet if a match occurs. A maximum handover number (MHN) in the packet will prevent it from being propagated for very long distances. This feature is also used in all other routing algorithms. The amount of storage that a repeater requires for this purpose is determined by the number of bits of the identifier and the MHNs which will be used; the latter is proportional to the size of the PRNET (number of stations and repeaters).

5.3.4 Remarks

Making the terminal (or terminal interface) transparent to the type of routing used will enable changes in the routing after an operating system is implemented and communicate it to repeaters without the necessity of modification in the terminal. It will allow use of the same terminal with different PRNETs that may use different routing algorithms. The implementation of this requirement is in the search procedure and the packet format.

NOTE

> It is important to make the terminal (or terminal interface) transparent to the type of routing used.

The directed and undirected routing algorithms can be implemented without a terminal search if such a feature becomes desirable. The routing algorithms will be software implemented. It is not expected that the control and management programs will be implemented in the stations and repeaters in the first experimental system. Furthermore, the first model repeater will be limited and will not contain all of the routing algorithms to be tested. Consequently, the repeater must be designed so that routing algorithm changes can be readily implemented. Repeaters should contain a hardwired fixed unique ID, which can also be used for routing when using nonhierarchical labeling. Repeaters are software associated with one station (and possibly an alternative) in the hierarchical labeling algorithm, and not associated with a particular station in the other routing algorithms outlined.

5.4 ACKNOWLEDGMENT SCHEMES

The acknowledgment scheme has particular significance in the PRNET because of the broadcast feature and the limited capability of the repeater for processing and storage. The following acknowledgments will be used:

a. End-to-end acknowledgment (ETE Ack) between station and terminal to ensure message integrity. The frequency and precise meaning of the Ack depends on the particular protocol used, and is part of the protocol.

b. A hop-by-hop passive echo acknowledgment (HBH Echo Ack) along the path. When device I transmits a packet, it waits a sufficient time to allow devices that receive the packet to repeat it. When any of these repeats the packet and the packet is received by device I, it considers it as an Ack. The Ack test includes a unique identifier of the packet and the maximum handover number (MHN). If the receiving device is an end device (terminal or station) it sets the MHN to zero and repeats the header to Ack devices that store the packet. Note that the HBH Echo Ack is nondirected and independent of the path travelled. This Ack simplifies the repeater program since it need not construct a specific acknowledgment for each packet it correctly receives.

5.5 FLOW CONTROL AND NETWORK MANAGEMENT

The various types of control packets suggested for implementation are outlined. The objective of the controls is to overcome traffic congestion and device failures. The various control procedures that will use the packets outlined are the subject of extensive testing and experimentation in the experimental system.

5.5.1 Local Controls To Overcome Traffic Congestion

The terminal search procedure controls the blocking level of terminals. The parameters in the procedure should be software selectable. These include:

a. The maximum number of times a search packet (SP) is transmitted

b. The interval of time over which the rescheduling of the SP is distributed

c. The procedure for sending a response to search packet (RSP) by the repeater or station.

The maximum number of transmissions (MNT) of a packet by all devices is another local control that should be software selectable. The maximum handover number (MHN), although not local, confines the propagation of the packet to a subnet, and thus controls the congestion level.

5.5.2 Station-Repeater Control Packets

The objective of these packets is to control traffic congestion, to preserve repeater power, and to overcome problems of repeater failure. There will be a possibility of using multiple addressing for these control packets. In this case, the station will transmit one packet to be propagated to all repeaters. The handling of the various control packets by repeaters will be discussed in another section. The control packets to be implemented are:

a. S→R Turn Off – will be used for controlling connectivity, particularly on the critical hop. A repeater that is turned off should receive all packets but respond only to a predetermined set of control packets, such as two.

b. S→R Turn On

c. S→R Replace your set of parameters by the set received. This will be used for replacing the following parameters:

   1. Time unit for sensing the channel

   2. Time interval for rescheduling

   3. MNT, MHN

   4. Power level to be used.

Pers about security or spoofing?

d. S→R Replace your RAM between locations X and Y by the information received. Will be used for replacing routing algorithms and reloading other repeater programs. This control packet can also be used for reloading repeaters when the bootstrap program at the repeater is activated and a packet to that effect is transmitted to the station. It is assumed here that the repeater may not have the capabilities and the backup programs to reload itself. This, however, should be further analyzed and the efficiency of reloading from the station evaluated.

e. S→R, Transmit to me the content of memory between locations X and Y. Will be used for collecting repeater measurements and for diagnostics.

f. R→S, A control packet which indicates that the repeater power is below some threshold.

g. R→S, A packet to station indicating some (or any) error that the repeater encounters.

Some of the control packets outlined will have a high priority. Packets from station to repeaters will always have an indication whether an acknowledgment is required. The station will have data files that will contain all updated labels and parameters of repeaters that will be used by the control algorithms. Organization in the station will be discussed later.

5.5.3 Station-Terminal Control Packets

The station will keep a file of active terminals in which the state of communication of each terminal is recorded. If an event (associated with a terminal) occurs that is not anticipated, special control packets will be used to resolve the problems. The following control packets will be implemented:

a. S→T, are you alive? Will be used when a packet from the terminal is expected and has not been received within a preassigned period of time. Another application is to make the inquiry before dropping information packets (IPs) after several times of reactivation - it may be a result of high priority.

b. S→T, Wait, everything is O.K. Will be used by a station when response from PTP net is slow and it receives another copy of IP from the terminal (which reactivated its IP when not receiving the ETE Ack from station).

c. S→T, Destination address (or PTP net) went down.

d. T→S, I depart from the system. Can be used when terminal departs from the system before completing communication. This packet can possibly be propagated to the destination address.

5.6 INITIALIZATION AND LABELING

The required algorithms are outlined in this section.

a. An algorithm for collecting the initial information by the station of repeaters and other stations in its area (e.g., connectivity). It is assumed that repeaters have a hardwired fixed ID, and a simple routing algorithm (to be determined) in its ROM.

b. Algorithms in the station for processing above information, determining repeater labels, and possibly negotiating with nearby stations concerning the division of responsibility.

c. Algorithms for transmitting the labels to repeaters and testing the network operation.

d. Algorithms to be used for reinitializing the network when a set of new repeaters or a station are added to an operating network.

5.7 SYSTEM PROTOCOLS

A listing of the protocols required is given below. The protocols are yet to be developed. This development will require extensive experimentation in the test system.

a. Station-terminal protocols will be needed to handle terminals with different capabilities such as:

1. Unattended sensors and position location

2. Handheld terminals

3. Small computers.

The particular protocol to be used can be either negotiated or fixed as a function of the type of terminal when this is communicated to the station. Small computers may have to reserve storage at the station.

b. Station-station protocol is needed for communication as indicated before.

c. Station-IMP or/and TIP protocol.

5.8 PACKET FORMAT

A packet consists of three pain parts: A header, a checksum, and text that consists in turn of the message, security information, and overhead such as header and checksums for other networks. All sections can be variable in length. The only limitation is that the header come first and is no more than 16 words (16 bits each), that the checksum come last and is no more than 2 words (32 bits), and that the total packet length is no more than 128 words (2048 bits). The first 8 bits of the packet must specify the length of the packet in words. Figure 5-2 is a nominal packet design.

HEADER

Packet Length in Words	Header Length in Words	Packet Type	Indicators	Sequence Number	To or From Station
1 8	9 12	13 16	17 20	21 24	25 25

Hierarchy Level Pointer	Handover Number	Routing Sequence Label	Repeater Label for Term.	Terminal User ID	Destination
26 28	22 32	33 64	65 96	97 128	129 160

PACKET

Header	Text	Checksum
10 words	1-116 words	2 words
160 bits	16-1856 bits	32 bits

Figure 5-2. Nominal Packet Format.

5.8.1 Types of Packets

There are three main types of packets: information, control and initialization, and diagnostic and measurement. There are, as well, subtypes of control and initialization packets, and of diagnostic and measurement packets. Control and initialization packets include:

a. On/Off Packet. An off packet addressed to a repeater causes it to no longer transmit; it still receives, so it can be turned on. Turning it on reverses the process.

b. Choke On/Off Packet. A choke off packet addressed to a repeater causes it to no longer accept packets from terminals. This is used to quiet down a saturated system. A choke off causes the repeater to resume accepting terminal search packets.

c. Parameter Packet. A parameter packet addressed to a repeater causes the repeater parameters (such as label, maximum handover number, time out values, and maximum number of retransmissions) to be reset according to values placed in the packets text section.

d. Load Packet. A load packet addressed to a repeater causes code from the text of the packet to be read into the repeater's memory.

e. ETE Ack. ETE Ack is an end-to-end acknowledgment sent by station and terminals to acknowledge the successful transmission from terminal to station or station to terminal, respectively.

f. Search Packet. A search packet requests all devices of a type specified in the packet text that can hear the packet to send a response packet.

g. Response Packet. A response packet is sent in response to a properly addressed search packet and includes the label of the responding device (station, repeater).

There are three diagnostic and measurement packet subtypes:

a. Trace Packet. A trace packet can be sent by either a terminal or a station to a station or repeater, respectively. Upon reaching its destination, the packet is sent back to the originating device. Statistics and routing information are collected in both directions and stored in the packet text.

b. Dump Packet. A dump packet causes portions of an addressed repeater memory to be copied into the text of a packet and sent to the originator. The information dumped can be statistics, data, or code.

c. Repeater Trouble Report. A repeater trouble report is sent by a repeater to a station if the repeater detects that it is about to become inoperable, e.g., battery power low or error interrupt in processor.

It should be noted that the on/off, the choke on/off, and the parameter packet are all special cases of the load packet in that they merely load new values into device memory. Similarly, the basic dump packet can be specialized to many differing diagnostic and measuring functions.

5.8.2 Packet Header

As far as hardware design is concerned, the header is variable in size and format except that: it is an integral number of words (a multiple of 16 bits), it is less than 16 words in length, and the total packet length is less than 128 words (2048 bits). Initial software will assume the nominal header configuration of figure 5-2; but, for various experiments, the packet format may be modified.

The fields of the header are:

Bits	
1-8	Packet size in words
9-12	Header length in words
13-16	Packet Type
0000	Information Packet
0001	ETE Ack
0010	Search Packet
0011	Response Packet
0100	Trace Packet
0101	Dump Packet
0110	Repeater Trouble Report
0111	Unused
1000	Load Packet
1001	Parameter Packet
1010	On Packet
1011	Off Packet

1100	Choke Off Packet
1101	Choke On Packet
1110	Unused
1111	Unused

Packets involving loading memory have a 1 in the high order bit.

17-20	Indicator Bits
Bit 17 0	Indicates directed routing
1	Indicates that packets are to be accepted by all repeaters closer to the station than the sender for packets to the station and by all repeaters away from the station for packets originating from the station.
Bit 18 0	Indicates ETE Ack expected
1	Indicates ETE Ack suppressed
19-20	Used to designate up to four protocols
21-24	Sequence numbers for packets
25	0 for packets to station; 1 for packets away from station
26-28	Level in repeater hierarchy
29-32	Handover number. Packet discarded when this reaches 0.
33-64	Routing Sequence Label consisting of eight fields corresponding to levels in hierarchy of 4 bits each
65-96	Repeater Label of repeater associated with the terminal
97-128	Terminal user ID
129-160	Destination descriptor.

Device addresses and labels consist of 32 bits, of which the last two are special. If the last bit is 2, every device that is checking the address to see if it is its own, takes it to be. In other words, the address is to "all." If the next to last bit is 1, the address refers to the fixed (hardwired or PROM) address of the device. If it is 0, the reference is to address labels assigned by the system. There are three 32-bit address fields in the packet: the routing sequence label, the terminal's repeater label, and the destination field.

5.8.3 Checksum

The last two words (32 bits) of each packet contain the checksum for maximum 32-bit cyclic error checking code.

5.8.4 Packet Size

The total packet size can be any multiple of 16 bits up to 2048 or 128 16-bit words. The header can be any multiple of 16 bits up to 256 bits. The last 32 bits are reserved for checksum and the first 8 bits for the packet length in words, so that hardware checksum calculation can be accomplished. The nominal packet design depicted in figure 5-2 has a 160-bit or 10-word header. Due to the nature of the ALOHA process, shorter packets will receive higher priority.

5.9 LOGICAL OPERATION OF DEVICES

5.9.1 Processing and Response of Devices to Packets

In the first implementations of the packet radio system, devices (repeaters, stations, and terminals) will have the majority of their logic for protocols, routing, and flow control implemented by programmable microprocessors. A large portion of the experimental program will be devoted to evaluating various protocols and routing and flow control disciplines. The "basic logical functional" capabilities of the devices must be sufficient to support the evaluation program. These basic logical functions can be thought of as being implemented in read only memory (PROMs), and should not vary appreciably in the experimental program. Thus, they must be quite general. More rapidly changing logic can be loaded into RAM remotely using the basic functional capabilities. Modification, testing, monitoring, and software maintenance must be possible from both stations and terminals.

5.9.1.1 Repeater Response to Packets

A packet is said to be addressed correctly for a repeater if:

a. The "all" bit (64) is set

b. The "undirected routing" bit (17) is 1; and the packet has hierarchy level greater than the level of the repeater for packets to station (bit 25 = 0) and less than the repeater level for packets away from the station (bit 25 = 1)

c. The directed routing bit (17) is 0 and the repeater is on the packet's routing sequence in the proper direction (to or from station).

A packet is "specifically addressed" to a repeater if bits 65 through 96 contain the repeater's label, or if bit 96 contains a 1.

A packet is repeated by:

a. Adding the packet to the Echo Ack queue

b. Decrementing the handover number

c. Inputting the hierarchy level of the repeating device

d. Transmitting the packet until an Echo Ack is received or the maximum retransmission number is exceeded.

A packet is accepted by a repeater if it is a priority packet or there is an empty buffer and if.

a. The packet is addressed correctly

b. The repeater is on and its choke is off, or the packet has priority; or the repeater is on and the packet is not a search packet; or the packet will be accepted if it is an Echo Ack (that is, it matches a packet in the repeater's Echo Ack queue), in which case the original transmission by the repeater was successful for one hop and the packet is dropped from the queue.

If an accepted packet is not specifically addressed to the repeater, it is repeated if the handover number is still positive. For trace packets, the trace information is appended before repeating.

If the accepted packet is specifically addressed to the repeater, the following actions are taken for each of the different types of packets:

a. Information. Not applicable.

b. On/Off. Repeater turned on/off.

c. Choke On/Off. Choke turned on/off.

d. Parameter. Parameters from text loaded into repeater.

e. Load. Code from text loaded into repeater.

f. ETE Ack. Not applicable.

g. Search. A response packet is sent containing the repeaters label in bits 65 through 96.

h. Response. Not applicable.

i. Trace. Information appended to text and the return packet for the station is started.

j. Dump. Memory locations specified in text copied into text.

Finally, if specifically addressed packets have the ETE Ack bit (18) set to 0, an ETE Ack is generated.

5.9.1.2 Station Response to Packets

A packet is addressed correctly to a station if bit 25 is 0, indicating the packet is to a station and the first 4 bits of the routing sequence label corresponds to the station.

A packet is accepted by the station if:

a. The packet is addressed correctly and there is a buffer free, or the packet has priority

b. If the packet is an Echo Ack of a packet in the station's Echo Ack queue.

Actions taken for the following packet types are:

a. Information. Information is read into station and ETE Ack is generated if bit 18 is 0.

b. ETE Ack. Corresponding packet(s) are considered to have been successfully transmitted ETE.

c. Trace. If the trace is originated by a terminal, information is added and the packet is sent back to the terminal. If it was originated by the station, the trace is complete.

d. Load. Text is loaded into station core according to format specified in text. ETE Ack is sent if requested.

e. Dump. Locations in core are loaded into text and the packet is sent back to the originator. If dump originated by station, dump is successful.

f. Search. A response packet is sent containing the station's label in bits 65 through 96.

5.9.1.3 Terminal Response to Packets

A packet is addressed correctly to a terminal if bit 25 is 1, indicating a packet heading away from a station, and the terminal user ID (bits 97 through 128) is correct or if bit 128 is a 1.

A packet is accepted if:

a. It is addressed correctly and either there is an empty buffer or the packet is a priority packet

b. It is an Echo Ack to a packet in the Echo Ack queue, in which case the packet is flushed from the queue and the corresponding transmission is considered successful for one hop.

Actions taken for the following packet types are:

a. Information. Information is read into the terminal and ETE Ack is generated if bit 18 is 0.

b. ETE Ack. Corresponding packet(s) are considered to have been successfully transmitted ETE.

c. Response. The repeater label in bits 65 through 96 is stored and information can now be sent.

d. Trace. The trace is complete and information can be read from text.

e. Load. The information in the text is loaded into the terminal interface memory according to a format in the text. An ETE Ack is sent if requested.

f. Dump. Information from the interface memory is read into the text according to a format in the text, and the information is sent back to the station. If the terminal originated in dump, it is succesful.

Other packet types are not relevant for the terminal.

5.9.2 Basic Storage Structure in Devices

In order to support the basic functions described in the previous paragraphs, a minimum amount of data structure must be maintained in the devices. Depending on the protocols, routing, and flow control used, additional data structures will be necessary.

a. Basic Repeater Data Structure

1. Packet Buffer(s). Buffers for packets being processed or awaiting processing

2. Echo Ack Queue. Stores packets waiting for Echo Ack

b. Basic Terminal Data Structure

1. Packet Buffers

2. Echo Ack Queue

3. ETE Ack Queue. Stores packets awaiting ETE Ack

c. Basic Station Data Structure

1. Packet Buffers

2. Echo Ack Queue

3. ETE Ack Queue

4. Repeater State Array. Keeps track of the current state of each repeater, e.g., labels and MHN's

5. Active Terminal State Array. Keeps track of active terminals

6. External Packet Buffer(s). Stores packets awaiting acknowledgment from external networks.

(Polarity)

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Section 6

Communication Link Design

6.1 RF CONSIDERATIONS

The packet radio network concept was originated to meet the requirements for more efficient and rapid communication from mobile digital terminals to central computing resources. Although there may be other possible means to interconnect mobile users, the radio channel seems to be the only practical one. Yet, the radio channel places severe constraints on the system design, particularly when considered in light of the portability and mobility of the terminals, the peak data rate requirements of terminals and computers, the limitations of state-of-the-art hardware, and the limited available radio frequency resource. what? problems

6.1.1 Propagation

The frequency selected for the packet radio repeater will lie in the 1 to 2-GHz range. The network is required to operate in urban areas with high rise buildings, as well as in suburban and rural areas such as jungles and deserts. Propagation in these topologies is highly variable, and although a great deal is known about these channels, some detailed knowledge is still being gathered. Appendix B.2 describes a measurement program to obtain information specifically oriented to help in the design of the repeater. Past measurements and initial results from this program have been used to model the channel and contribute to the rf design. Future measurements will be used to suggest refinements and modifications. Motivate freq. band.

The propagation channel introduces a random attenuation and phase shift to rf signals. In addition, the channel can severely disturb an rf signal. These effects are all due to the fact that a signal travels from one point to another over multiple paths. Usually, there is a direct or line-of-sight (LOS) path with minimum attenuation and delay, although this path may not exist in severe environments such as jungles or cities. Often, there are additional paths due to the fact that the signal may be reflected from one or more intervening objects. The additional paths have delays and attenuation in excess of the LOS path, so that a transmitted pulse may be received as a set of pulses with random delay, amplitude, and phase.

An example of multipath propagation is shown in figure 6-1. The pulse distortion here is very apparent. This picture was taken in Palo Alto using the measurement equipment described in appendix B.2.

Figure 6-1. Example of Multipath Propagation.

The random attenuation and distortion have two effects. Random attenuation means that coverage areas for repeaters will be random. Two receivers within a few feet of each other may experience such different signal levels that one may operate without errors, while the other may be unable to operate at all. Coverage areas must be described probabalistically, and the rf design must take this randomness into account. For the initial experimental network, the terminals will be required to move whenever a very low signal level is encountered. Experiments with redundant repeater coverage and various other diversity mechanisms are planned to improve the design in this respect.

The signal distortion introduced by the multipath channel places a limit on the bit-rate which the channel will support. The delay spread of the channel is a measure of the distortion introduced. It is determined by the 3-dB points on the channel impulse response. An example is shown in figure 6-1. If this spread is greater than the duration of one signaling element (baud), which is usually a single bit, then intersymbol interference will result, and errors will occur even at high signal-to-noise ratios.

Various schemes have been devised to combat multipath effects, and many are considered in appendix B.1. Only the most complicated are effective in the random time-varying environment envisioned for the portable terminal. Some of these may be experimented with as the program continues; however, it initially appears that peak power and desired repeater coverage will limit the bit rate to values less than the propagation limit (see appendix B.1).

The mobility of the terminals, combined with the space variability of the channel may impact the rf design; however, additional information is needed in this area. The measurement program (appendix B.2) will collect much of this information. The high bit rate (100 kBps) the maximum speed (100 mph), and the nominal packet length (100 kBps) will combine so that the terminal may move as much as 5 feet during one packet. This is 10 wavelengths at 1.6 GHz. Severe fades may be encountered in much shorter distances; hence, this problem is one that must eventually be solved. The initial experiments will be made with much slower terminals, and several means to solve the higher speed terminal problem will be explored as data becomes available These will include diversity schemes, shorter packet lengths for mobile terminals, and error correcting coding schemes.

6.1.2 Noise

There are at least three major types of noise in this band. These are characterized by their nature as background (or Gaussian), impulsive (or non-Gaussian), and interference. The latter will be considered as a part of the coexistence problem discussed in paragraph 6.1.3.

In the absence of other noise and propagation effects, the background noise places a fundamental limit on the capacity of an rf link to support communication. This limit depends on the average power and bandwidth available and is commonly called Shannon's bound. The application of this bound to packet radio is discussed in appendix B.1. For several practical reasons, this bound cannot be used as a design objective; however, it does supply a measure of design quality.

Link power budget and repeater LOS coverage calculations are based on the background noise level. In the 1- to 2-GHz band, this noise is primarily of thermal origin and may be taken as thermal noise at 20°C. Such noise is assumed to have uniform spectral density of -173 dBm/Hz and to have a Gaussian amplitude distribution.

The primary impulsive noise in the 1- to 2-GHz band appears to be derived from automobile ignition spark discharges. Hence, it varies with population density. Other sources of impulsive noise are also manmade, such as arc-welders, electric trains, and ac power distribution systems. All are population density dependent.

Impulsive noise is not generated at a high level, so that it is only effective at short range. For example, a terminal on a main city street, or near a freeway might experience noise impulses exceeding the thermal noise by 60-to 80-dB; but a repeater, several hundred feet above the street on a tall building, might experience impulses of only 30 to 40 dB above thermal noise, and a repeater on a mountain in a suburban or rural area might experience only background noise.

The design power budgets for the initial system have included a 10-dB noise margin to accommodate typical suburban noise impulses, and the initial system experiments will be accomplished in such an environment. It is clearly not desirable to limit repeater coverage so that all impulses can be overpowered by the signal. This would reduce coverage by factors of several million in worst-case situations. Instead, provision has been made to implement and experiment with error-correcting coding techniques. Such techniques will depend on the detailed time-statistics of the noise impulses which are being collected (appendix B.2).

6.1.3 Repeater Power Budget

why?

Satisfactory performance of the repeater-terminal or repeater-repeater links of the network depend upon the receipt of adequate signal power to overcome the noise at the receiver. Signal power received will be adequate so long as the energy per bit to noise density ratio does not drop below about 13 dB.

The signal power received will depend upon system parameters such as transmitter power, and transmitter and receiver antenna gains which are fixed by the system design. It will also depend on parameters such as the antenna heights above surrounding terrain, the nature of the intervening terrain, and the topology of the receiver location. All of these can vary greatly within a repeater network, and propagation loss may vary significantly as a terminal moves only a few feet. The background noise level is less dependent on system parameters, but also will vary with receiver location.

Because repeater coverage is so terrain dependent, it is possible only to present "typical" repeater range curves. Such curves are shown in figures 6-2 and 6-3. Figure 6-2 can be used to estimate the median range for satisfactory performance when the receiver is in a rural location and figure 6-3 for an urban location. Range will depend on the bit-rate and background noise, as well as antenna heights. These figures have curves for 2-bit rates (100 kBps and 500 kBps) and various antenna heights, assuming one antenna is always at 1.5m for a 100-kBps rate, and one antenna is

Figure 6-2. Typical Repeater Range Curve, Receiver in Rural Location.

Figure 6-3. Typical Repeater Range Curve, Repeater in Urban Location.

always at 200m for a 500-kBps rate. Repeater design parameters of this design plan have been used with propagation loss models to arrive at these curves, as explained in appendix B.2, which also explains how other antenna heights can be used.

To better understand these curves, consider two examples of application.

Example 1: Typical Urban Repeater-Terminal Range.

A typical urban repeater might have an antenna height of 50m. The terminal antenna height probably would not exceed 1.5m, and the terminal background noise would be about 15 dB above thermal. Using figure 6-3, and the 100-kBps scale, we find that the median repeater range is about 3.5 km.

Example 2: Repeater-Repeater Range in a Rural Area.

In this case, we might expect both repeaters to be located on mountains, perhaps 200m high. The bit rate will be 500 kBps, and we expect only thermal noise at the receiver. Under these conditions, we find that the median range will be 45 km.

These curves will be useful in estimating the minimum number of repeaters required to cover a given area, and in choosing repeater locations; however, redundancy of some form will be necessary to ensure uniform coverage.

6.1.4 Coexistence

A major rf consideration is the fact that the rf spectrum is a limited resource. Any new communication system must be designed in light of its impact on existing users, and must be designed to use the spectrum as efficiently as possible.

important

In the past, spectrum use has been planned by assigning frequencies to specific users, and requiring that they use as little bandwidth as needed to accommodate their peak data rate. Occasionally, nets were assigned to share a frequency, and this improved the efficiency; when the frequencies are not being used, they are unavailable to anyone else, and efficiency is reduced. Because of the random nature of propagation, geographical reuse rules must be such that some frequencies are never used in some areas, and additional capacity is lost.

The packet radio concept can help to improve spectrum utilization. Many users can be assigned to time share a single frequency so that the channel is more efficiently used. This concept is a major advantage and its implementation is central to the planned repeater.

Because of the geographical distribution of a packet radio network, the nature of the packet radio traffic, and the nature of other spectrum users, it is possible to design a network that will use part of the unused capacity available at frequencies assigned to other users, without affecting the other users significantly. This concept is controversial, and will require careful exploration; yet, it promises to make major inroads into the spectrum usage problem if it can be successfully implemented.

Two alternative designs have been suggested to accomplish this latter coexistence goal. The design described in this plan uses unused capacity by implementing a spread-spectrum signaling scheme so that the energy density seen by other users is very low, and so that the effect of other users on the packet radio network is reduced by the filter/signal mismatch. The scheme initially implemented may be made more efficient as the program progresses by multichannel extensions and error-correcting code implementations, and the equipment will be designed so that such modifications are readily possible. An alternative design involves a slow frequency-hopping scheme in which assigned, but locally unoccupied channels, are used by the packet radio net, and locally-occupied channels are avoided. This scheme is described in appendix B.3. It is simple enough so that the experimental network could be implemented in this manner if extreme difficulties occur in the presently planned design. A third alternative would combine the best features of both the spread-spectrum and slow-frequency-hopping scheme to overcome coexistence problems which might overwhelm either system. This alternative will be explored in parallel with the implementation of the present design.

The coexistence problem has two aspects. The system must avoid interference from other users, and it must avoid interfering with other users. The specific nature of the problem depends on the specific community of users coexisting. Preliminary experiments with radars (see appendix B.4) suggest that it is possible to coexist with even such difficult users if the repeater coverage is sufficiently small (necessitated by the radar receiver sensitivity to low power density signals) and error correcting codes are used (necessitated by the high peak-power radiated by the radar). Coexistence in other user communities should be much simpler and exploration of this issue will be a major goal of the program.

6.2 BASIC RF LINK DESIGN

The basic rf link may be discussed in terms of the block diagram of figure 6-4. In this simplified picture, the source generates a digital message (which is best thought of as a packet). The packet is encoded and converted to an analog waveform by the encoder and modulator.

The analog waveform is frequency translated, perhaps filtered, amplified, and radiated by the transmitter. The transmitted signal is distorted by the channel, and various types of noise are added, so that the received signal is a random waveform correlated to the transmitted waveform, but not a precise replica. The receiver demodulates and decodes the received signal in an attempt to reproduce the original message.

Thus, the important design elements available to control the performance of the link are the modulation scheme, the encoding scheme, and to some extent, the choice of frequency of operation.

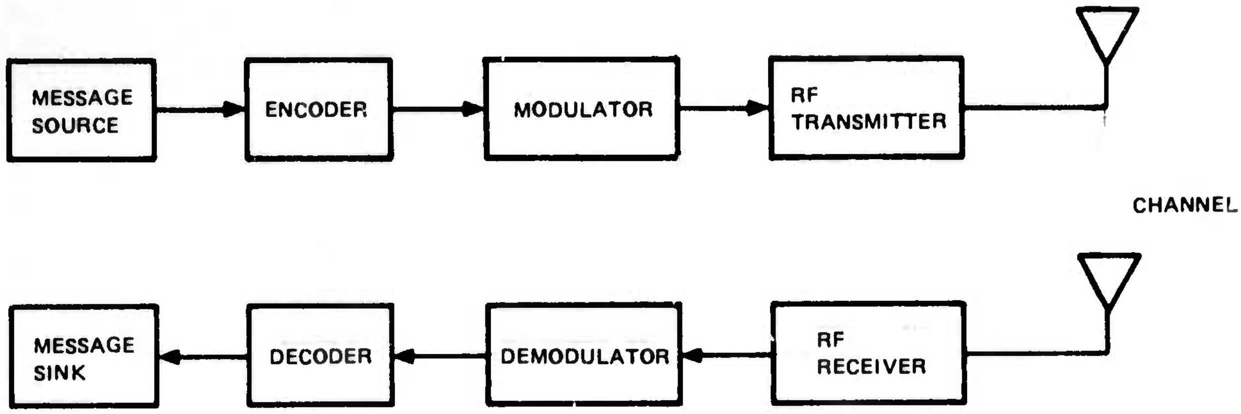


Figure 6-4. Basic Link Block Diagram.

6.2.1 Modulation Scheme

Three modulation schemes are described below briefly. Each meets the two basic requirements that the scheme must use transmitted signal energy efficiently, and it must support a basic bit rate of 100 kBps. They differ in several other properties, all deemed desirable for the repeater design.

Scheme A. In the first scheme, the 100 kBps data is used to differentially-biphase modulate a spread spectrum waveform with a 20-MHz bandwidth.

Scheme B. In the second scheme, the 100 kBps data is split into five channels of 20 kBps each. Each channel is used to bi-phase modulate a spread spectrum waveform with a bandwidth of 4 MHz. The five spread-spectrum waveforms may be selected from 10 possible channels

Scheme C. In the third scheme, the 100 kBps data is used in a quadratic differential biphase modulator to modulate a sine wave chosen from any one of 300 frequencies, separated by 100 kHz.

The desirable properties in which these schemes differ are defined below.

1. Allow Investigation of Coexistence Issues

   It is important that any scheme for the initial repeater support experiments with coexistence. The broad-band schemes (A and B) both provide such capability, but Scheme C does not, unless it is combined with the slow frequency-hopping channel access scheme of appendix B.3.

2. Easily Implemented

   Although it is not a prime requirement that the scheme be easily implemented, it is very desirable in the first repeater network because of the primary emphasis on learning about such networks. Once the initial experiments are complete, perhaps the investment in special components to improve the network will be justified, or perhaps other approaches will be discovered. Scheme C is easily implemented. Scheme A is not much more difficult, except that state-of-the-art in matched filters will be required. Scheme B is moderately

difficult because the resulting waveform would be amplitude-modulated, and a single Class C power amplifier could not be used.

3. Use Frequency Resource Efficiently

Discuss differently

Although all three schemes occupy the same bandwidth allocation (roughly), schemes A and B use much more bandwidth than Scheme C. If Schemes A and B caused no more interference to other users or provided the same range coverage in the presence of other users, then the bandwidth usage would not be an issue; however this is not the case. Clearly, Scheme C can operate as a single-channel scheme and coexist with any mix of users in the 1- to 2-GHz band. Only as multiple channels are introduced as it reasonable that schemes A and B might perform as well as scheme C.

4. Provide A Measure of Security or Privacy

All three schemes are equally easily detected and jammed by an enemy with a stolen receiver and transmitter; however, Schemes A and B have the potential to provide some measure of security if modified to psuedorandomly select a spread-spectrum waveform. Such modification would greatly change the implementation difficulty and performance of either scheme. Scheme C is not modifiable to provide low detectability, but could be used in a bit-by-bit frequency-hopping mode at a loss in performance.

The scheme chosen for the initial repeater is Scheme A. This reflects our emphasis on rapidly exploring the packet radio issues so that a major improvement can result quickly. Ultimately, Scheme B or some combination of B and C may result, but Scheme B would unduly complicate the experimental repeater, and Scheme C would not provide the opportunity to explore the coexistence issues.

why not allow privacy work in this area

Thus, the modulation scheme selected is a spread-spectrum signaling format. The digital data will be used to differentially biphase modulate a spread-spectrum carrier. The spread-spectrum carrier will be generated using a maximul length sequence generator to minimum shift key (msk) modulate a sine wave.

Detailed block diagrams of the implementation scheme for the modulator and demodulator are discussed in section 8. Demodulation is accomplished using a matched filter differentially coherent scheme.

The performance of such a scheme in Gaussian noise depends on the received energy per bit to noise power density ratio (E_b/N_o). A curve of bit error-rate vs E_b/N_o is shown in figure 6-5, assuming perfect bit synchronization.

The spectrum of an msk signal has a smooth variation with no sidelobes, so that out-of-band power can be controlled without transmitter filtering. The normal bandwidth is determined by the bit rate and the spread factor, and is given by twice their product.

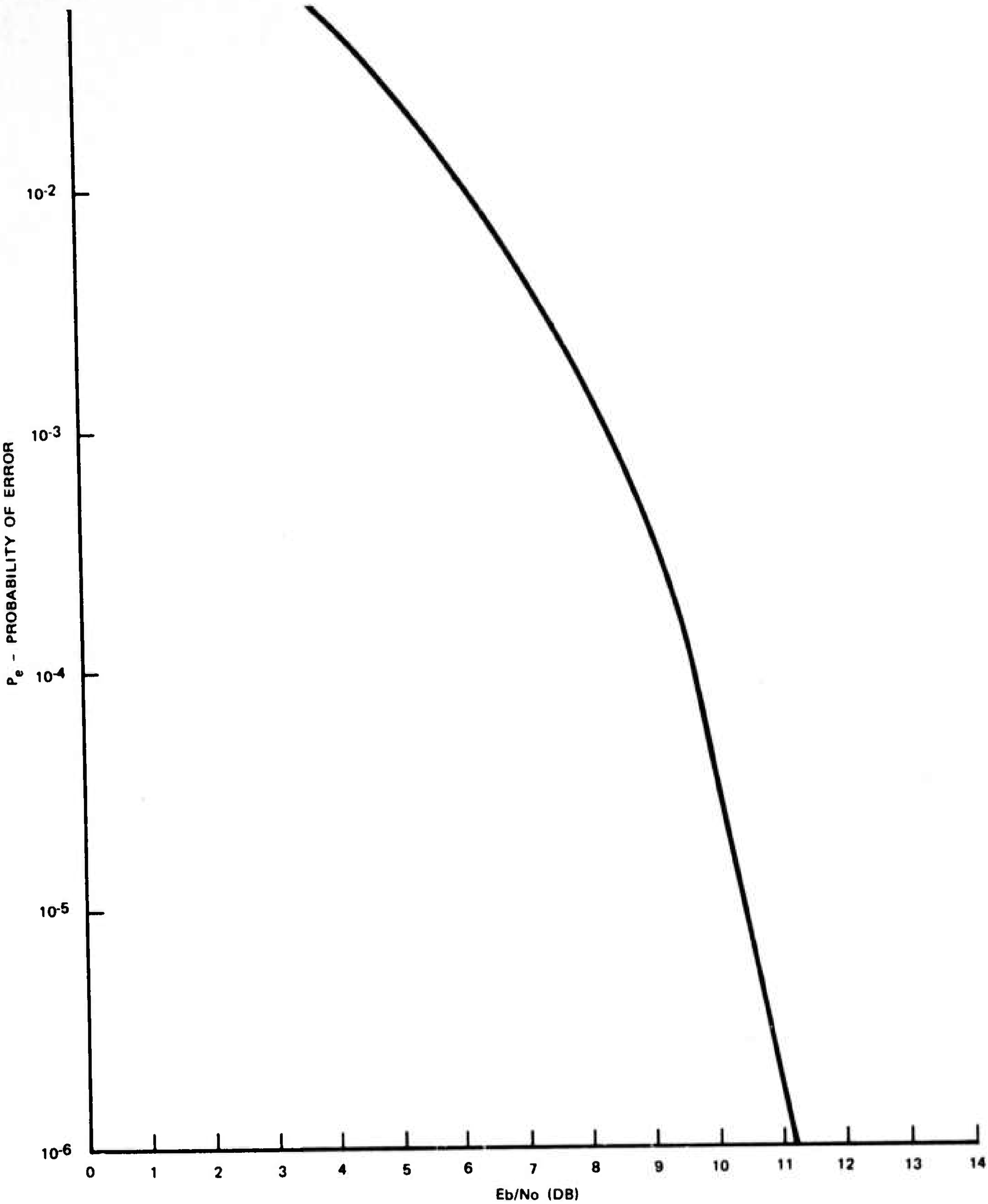


Figure 6-5. Curve of Bit Error Versus E_b/N_o.

Two bit rates are planned. The bit rate used for the terminal-repeater link will be 100 kBps. Using a spread factor of the order of 100, the nominal rf bandwidth will be 20 MHz. The repeater-repeater links will experience less noise and less multipath. For network efficiency, the initial repeater design will allow a 500 kBps bit rate with a spread factor of 20, resulting also in a 20-MHz nominal rf bandwidth.

6.2.2 Coding

[illegible]

The initial repeater design will contain an error-detecting coder. The coder will generate 32 parity bits per packet using a cyclic convolutional coder. The decoder will use the same convolutional coder to generate a syndrome and check for errors. So long as bit errors are random, such a coder should assume that the probability of undetected errors in a packet is less than 2^{-32}. Loss of synchronization is not readily detected by such a coder unless steps are taken to destroy the cyclic nature of the code. Various approaches to this task are being studied and one will be implemented in the repeater.

Such a technique will detect errors caused by impulsive noise or interference as well as random errors. However, detection is probably not enough in the former case. It is possible that in urban areas, noise impulses exceeding thermal noise by 60 to 80 dB will occur with such frequency that virtually every packet will experience at least one impulse. In an rf environment containing several radars, each packet might experience two or three errors. Thus, in these cases, very few packets would be accepted and the channel capacity and throughput would be very low. Contrast this to the Gaussian noise, random error case where the probability of bit error is 10^{-5} by design power budget. Roughly 1 in 100 packets will be rejected due to a detected noise error.

It is probable that some form of error-correction coding will be required as network experiments are extended to urban areas and coexistence experiments are undertaken. Parallel studies to determine impulse statistics and to explore possible error-correcting coders are underway and the results will be used in the repeater.

6.2.3 Synchronization

Three forms of signal-synchronization are possible. There are packet synchronization, bit synchronization, and carrier-phase synchronization. Packet synchronization is necessary to ensure proper decoding of the bits and to properly frame the packet for digital operations on the header and the text. This will be accomplished by transmitting a special spread spectrum waveform, normally orthogonal to the carrier, but occupying the same band, for a duration of 6 bits prior to initiation of a packet transmission. The receiver will detect this waveform with a matched filter. This should ensure that sync will occur with a probability of >0.999, and false synchronization will occur with a probability of $< 10^{-6}$ at design power budget in Gaussian noise. The synchronization error should not exceed 1/10 bit rms when synchronization is detected. ?

Why?

10 MHz @ 100 = 100 kb

20 MHz @ 200 = 100 kb

Bit synchronization will be accomplished by phase-locking a clock to the demodulated data. It is important to have acquired bit synchronization by the time of demodulation of the first data bit following packet sync. This can be accomplished either by using the packet synchronization impulse to phase adjust a stable clock (assuming a stable transmit clock) or by delaying bit demodulation until enough data has been received to allow acquisition of bit synchronization from the data. The former approach requires stable clocks, the latter requires analog or multiple-level digital buffer storage. Both approaches will be studied, and the best will be selected.

Carrier synchronization will not be used in the repeater. Differentially coherent demodulation will be used so that carrier synchronization is not needed. Performance at the design power budget will not be significantly degraded because of the lack of coherent demodulation. (Approximately 1.5 dB is lost).

6.3 CHANNEL ACCESS SCHEMES

6.3.1 Single Channel Modes

The initial repeater should be designed to operate in three channel access modes, so that experiments with different access schemes are possible. The three schemes are referred to as ALOHA, Carrier Sense (CS), and Spread Spectrum with preamble synchronization (SS).

a. ALOHA Mode. When operating in this mode the repeater will transmit a packet whenever one is ready. The packet will be transmitted at a high data rate (500 kBps) if it is meant for a repeater. If the packet is not acknowledged within a (software-selectable) period, the repeater will retransmit. The throughput from terminals to repeater in the absence of network signals (such as repeater-repeater) theoretically saturates at one-half of the bit rate. Other access schemes exceed this theoretically; however, in network operation the improvement of other modes may not be worth the loss of simplicity.

b. Carrier-Sense Mode. When operated in this mode, the repeater will first determine that the channel is unused, then transmit the packet as in the ALOHA mode. Parameters of this mode will be software-selectable. To implement the carrier sense scheme, it is only necessary to provide a "carrier detect" circuit and the logic to inhibit transmission whenever a carrier is detected. This scheme can more than double ALOHA capacity when all terminals can detect each other. Operation in a real network environment remains to be evaluated. Nb!

c. Spread Spectrum. The Spread Spectrum requires that the synchronization preamble, needed in any case for packet synchronization, be used to start a clock which samples the demodulator only at bit intervals.

   Theoretically, a second packet arriving more than two chips (200 ns) out of synchronization with the first will not interfere, and the channel capacity will be improved to exceed ALOHA significantly; however, high multipath is likely to make any improvement very slight. For successful operation, preamble synchronization and bit rate clock stability must be such that the sample is made near the peak of the matched filter output (which is only 200 ns wide). A

"sampling window" slightly wider can be used with a threshold circuit to relax the timing requirements somewhat at some increase in bit error rate, and loss in channel throughput. The availability of the circuitry for an Spread Spectrum mode will be needed in any case if multiple-channel operation is planned.

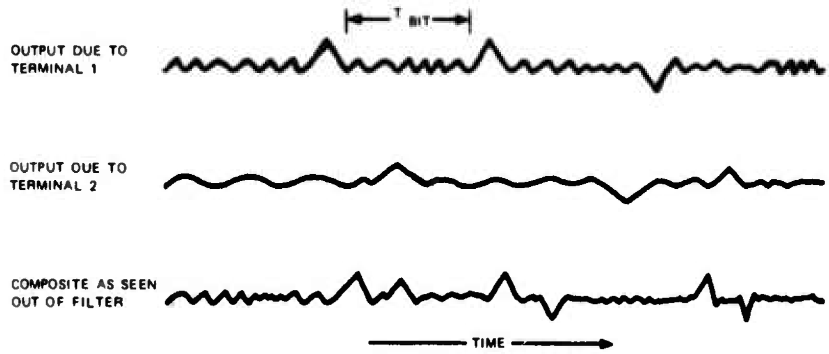
The repeater should be designed so that operation in each mode is software-selectable with software-selectable parameters such as retransmit time.

6.3.2 Multiple-Channel Modes

Must be capable of extending!

Although the initial repeater may not include implementation of multiple-channel modes, design should not preclude modification to provide for one or both of the following:

a. Multiple Time Channels. When operating in a low-multipath environment with power-controlled terminals, multiple-time channels can be used if the spread-spectrum code selected has low auto-correlation (aperiodic) sidelobe levels. A sketch of the output of the envelope of a matched filter receiver is shown as an example of two-channel operation:



These two channels can theoretically be separated by suitable time gates at bit intervals, initiated by synchronization preambles on each channel.

b. Multiple Code Channels. When operating in a high-multipath environment with power-controlled signals, multiple codes can be used to achieve multiple channels. This is accomplished with a separate matched filter for each channel (code). Because the terminals cannot be globally synchronized, each channel will cause some interference to the other, limiting the total number of channels. A separate modem must be provided for each channel. Whenever the transmitter operates, all channels are blocked at the repeater.

6.4 ALTERNATIVE ACCESS SCHEMES

The multiple-channel, dual bit rate, spread spectrum access scheme has been chosen to provide an acceptable compromise of performance factors; however, uncertainties exist in knowledge of the effect of propagation and practical hardware constraints. Another possible access scheme is discussed in appendix B.3.

Measurement and Testing

As the packet radio concept and models for this concept have grown, the need to perform field measurements on an experimental system has become clear. This need has several sources. The interaction of the radio channel, network protocol, user, and use are difficult to describe, much less model. Models for each subelement are necessarily simplified, and many unknowns enter into field operations. Finally, the equipment design problems are difficult and the system design tasks are even more difficult. Both require field verification. It has become apparent that an experimental system and a measurement plan are needed to explore the packet radio issues.

The experiments that can be performed and the measurements that can be made depend heavily on the experimental system design. Similarly, the design depends upon the measurement plan. This interdependence results in the necessity to iterate the process of system design and measurement planning. In this section, a first approach to a measurement plan is discussed. This plan will be used to design an experimental system to support the plan. In turn, the system design will influence the eventual plan.

Three types of measurements are described. These correspond roughly to the three anticipated phases of the system buildup. The first type of measurements involves communication link experiments and will be referred to the first phase of the experimental system when only a few rf nodes are available. These experiments will validate the rf link design, test rf equipment performance and design, explore coexistence questions, and validate propagation, noise, and modem/coder models. The results of these experiments will be used to modify and improve the link design and to explore important packet radio issues (such as coexistence) to the extent possible with a few rf nodes.

As the experimental system is expanded, more nodes are added, and the rf system is improved; then network experiments will be possible. Because this phase is farther in the future, many of the desired experiments are yet to be defined in detail; however, the measurement parameters and necessary facilities have been determined from network models and simulations. Once the equipment design has stabilized and network experiments have been used to modify and improve the network design, it will be possible to examine traffic patterns, network utilization, and operation of individual network elements under various uses and stresses. These experiments will require yet a third set of measurable parameters and facilities, and will be carried out during the third phase of the experimental system life when it will be possible to use the system to support limited operations with real or simulated users.

This preliminary plan is organized to first describe link-related, network-related, and user/operational performance experiments that the experimental system will support. The parameters to be measured are then listed for each class of experiment. Finally, the facilities needed to support the measurements are briefly summarized.

7.1 LINK-RELATED EXPERIMENTS

The link-related components are designed using models that relate bit and packet error rate to link parameters (such as propagation, noise, range, topography, and interference) and equipment design parameters (such as bit rate, modulation type, coding technique, and packet length). In addition, certain aspects of the access mode models are link-related. Many of these models have been validated by previous study and need not be tested again; however, several aspects of the communication-link problem are unique to the packet radio system and require additional testing for verification of design or determination of performance. These are emphasized in the measurement program.

The PR network will use modulation, coding, and access techniques that have not previously been applied to the rf environment in which the network must operate. Spread-spectrum msk signals have not been tested in multipath environments similar to that expected in the 1- to 2-GHz range in urban areas. High-rate digital communication systems have not been subjected to the type of noise expected in this environment, and new concepts of rf coexistence are being explored. These have all been reasons for the development of the mobile instrumented test facility described in appendix B.2. As presently configured, this facility consists of a transportable (truck-mounted) spread-spectrum transmitter operating with a 20- to 40-MHz bandwidth in the 1200- to 1400-MHz band, and a mobile (van-mounted) receiver, minicomputer, and digital recorder. The transmitter/receiver can be used to sound the channel and determine propagation conditions. The receiver also measures noise parameters. The minicomputer controls the receiver and records the data. (See appendix B.2 for a complete description.)

This facility will be modified so that the digital section of a repeater or terminal can be directly connected to the minicomputer. Packets and repeater status information will be sent back and forth. The resulting measurement capability will be used in the following experiments.

7.1.1 Error Rate Versus Range and Topology

As part of the packet radio program measurements of multipath, propagation loss and noise have been undertaken, and the resulting models have been used to aid in the design of the communication link.

The experimental facility will be used to validate the models as well as the resulting design. To accomplish this, simultaneous measurements of propagation conditions, noise, and link error rate are needed. The existing test set will be employed. The equipment in the van will be modified and connected to a repeater and/or terminal so that error rate measurement can be automatically recorded. The planned equipment setup is shown in figure 7-1.

The measurements will be made by selecting sites for the repeater and terminal that will expose the link to different propagation and noise conditions. The measurements currently being made will be used to select specific repeater and terminal locations. The terminal will be used to generate known messages, or bit patterns, and the repeater will pass the received patterns to the minicomputer. The computer will determine errors and record error statistics. Simultaneously, the propagation

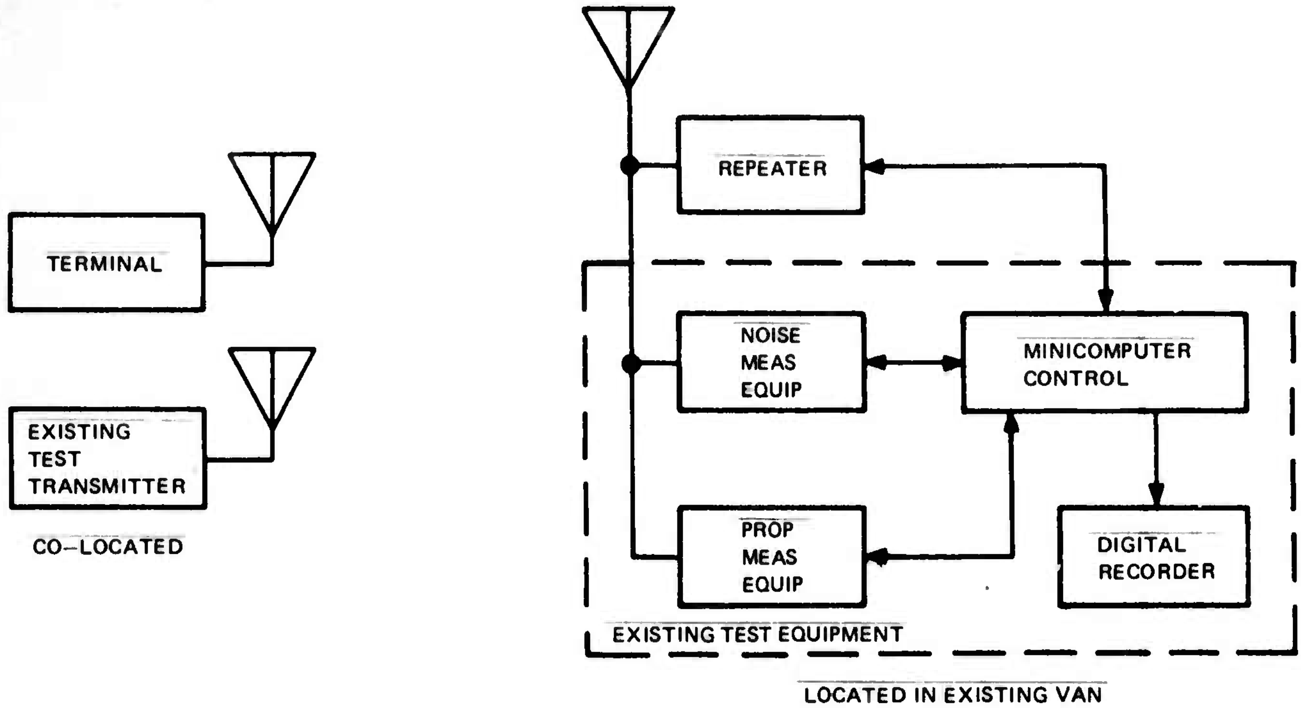


Figure 7-1. Diagram of Error-Rate Test Setup.

and noise statistics will be recorded for later comparison to the error measurements. The results of these measurements will be compared to theoretical performance predictions to validate the models and equipment design.

7.1.2 Coding Effects

Because of the existence of impulsive noise and the desire to coexist with other users, it will probably be necessary to employ error correction coding on the rf links. Several kinds of codes are candidates; and it will probably be impossible to predict performance accurately enough to select the best, so that field comparisons and measurements will be needed. If one is selected analytically, it will still be desirable to determine actual performance and the effect of parameter variations.

The test facility will be used in two ways to aid in coding experiments. When a complete coder/decoder is constructed, the test facility will be used to collect error rate data under different propagation and noise conditions as discussed in paragraph 7.1.1. More importantly, the facility will be used to simulate the decoder so that a wider variety of coding techniques can be explored. This is possible since the decoder is usually expensive to construct, but easily simulated on a computer.

7.1.3 Coexistence Measurements

A major goal of the PR program is to develop a network that will coexist with other users. To explore this issue and to demonstrate that a given design does indeed coexist, it is necessary (but not sufficient) to determine the extent of disruption caused by other users. It will be possible to use the mobile test facility to find other users by spectrum monitoring and to measure the effects of these users by logging error rates when co-users exist. These "targets of opportunity" will be supplemented by transmitters to simulate user environments as needed to explore the issues involved.

The other half of the coexistence coin involves interference by the PR network <u>to</u> other users. Some interference tests have been made using the existing test set and two operational radars. These tests will be repeated, and similar tests with other types of equipment will be undertaken. These tests will be performed, where possible, on targets of opportunity; however, in many cases it will be necessary to employ users simulated by sensitive receivers, or to take the PR repeater to a location where users exist.

7.1.4 Access Mode Experiments

Network throughput and delay depend on many variables. An important factor in both performance measures is the access mode used by the terminals and repeaters. Analyses of throughput and delay have modeled the users as an infinite population of Poisson sources, and have ignored the effects of noise and acknowledgment packets. Simulations have used finite populations, but other aspects of the simulations have necessarily been idealistic. Network experiments (discussed in paragraph 7.3) will be made to validate the network models, simulations, and designs; but it is also necessary to perform link measurements using a single repeater and many terminals to validate some aspects of the access mode models.

Several experiments are possible if the equipment is properly designed. For example, models suggest that the Carrier Sense mode is more efficient than the ALOHA mode so long as all terminals can hear each other; but as soon as terminals are "hidden," performance degrades. A field demonstration and measurement of this effect can readily be made if the equipment has both a Carrier Sense and an ALOHA mode.

In a different type of experiment, measurements can be made to determine the number of spread-spectrum channels that can simultaneously occupy a frequency band. These measurements can be made in lieu of, or prior to, building multiple-detector receivers in the repeaters.

7.2 NETWORK-RELATED EXPERIMENTS

Network-related experiments are briefly described in two categories: routing and flow control and network performance.

7.2.1 Routing and Flow Control

The following objectives describe routing and flow control.

a. Initialization and Labeling Programs. The objectives are to assess the efficiency of the programs, to develop new programs, and to estimate the times needed for network labeling and testing.
b. System Protocols. In the first experimental system, the emphasis will be placed on developing and testing a basic set of protocols for communication within the packet radio network (PRNET). The station will have (eventually) protocols for communication with other stations and with the PTP network; these will be the subject of future experiments. Several terminal-station protocols will be tested. The protocols must be tested in a one-hop system (i.e., terminals communicating directly with the station) and in a multihop system. Ideally, in developing a protocol, one should take into account the probability of successful transmission between the two communicating devices. When the above probability is low, one would tend to develop a more complex protocol to reduce the number of packet transmissions. Thus, terminal to station protocols will eventually be tested in a multihop multistation PRNET. The station must be tested when simultaneously communicating with several terminals, not all of which use the same protocol.
c. Routing Algorithms. The objective is to assess the efficiency of the routing algorithms developed in a field environment.
d. Control Procedures. The objective is to test the capability to overcome congestion and repeater failure by dynamically modifying the network configuration. This will be done by controlling the operating devices (on/off) and changing the operating parameters of devices.

7.2.2 Network Performance

Apart from the particular software used, the main parameter to be changed when estimating system performance is the traffic rate offered to the system. "Retransmission" is defined to be when a device retransmits awaiting an HBH Ack. "Reactivation" is when a device does not receive an ETE Ack and activates the packet for another sequence of transmissions.

a. Throughput. Considering the set of stations and the set of terminals as the end devices, the system throughput (in packets) is defined as the rate of information packets (IP's) that originated at stations and arrived at terminals, plus the rate of IP's that originated at terminals and arrived at stations. Some of the packets contributing to the value of throughput as defined above will be contributed by IP's that have been reactivated. Thus, one can speak of gross throughput as defined above and net throughput in which the rate of reactivated packets is not considered. The net throughput can also be defined as the summation of the rates of IP's that have been end-to-end acknowledged. To obtain a detailed observation of system performance, it is necessary to measure the gross and net throughputs. The difference between the two reflects the efficiency (or deficiency) of the routing and protocols.
b. Delays. The following delays will be measured:
   1. Time delay to initialize repeaters and test repeater-station network
   2. Terminal delay to identify specific repeater

3. Terminal delay to establish communication with station and to negotiate protocols
4. End-to-end delay for an IP
5. Terminal interaction delay as a function of the number of IP's transmitted and received. The interaction delay is defined as the time elapsed from terminal origination to departure.

c. Blocking and Loss. When a terminal does not successfully identify a repeater (or station) after transmitting an SP for the maximum number of times specified, it is considered blocked. In addition, under certain conditions, terminals will depart from the system without completing communication. This will contribute to additional system loss. The blocking and loss should be measured separately since the former indicates the difficulty in entering the system, whereas the latter reflects on the inefficiency of the routing.

7.3 USER AND OPERATIONAL EXPERIMENTS

During the later phases of the system life, it will be possible to perform many types of experiments with operational or experimental users to explore the interaction between the user and the system. Three examples of such experiments are outlined below.

7.3.1 Time Sharing

The experimental system can be set up to operate as a time sharing network to explore the interaction of such users and PR networks. The effect of network delay on user traffic, the ratio of terminal-generated to computer-generated traffic, and general network traffic patterns should all be measured. The effect of geographical distribution of user traffic on the network and the dynamics of network saturation should also be better understood.

To perform this type of experiment, the system should be deployed in an area where time-sharing users are readily available to help saturate the network. A geographical area large enough to support wide distribution of users in a variety of topologies should be chosen. The system should be set up with several repeaters and a station capable of acting as a time-sharing computer, or as a gateway to another time-sharing network such as the ARPANET. The ability to saturate different parts of the network selectively should be provided, and measurements of network performance and user reaction should be made.

7.3.2 Dynamic Deployment

A major application of the PR network to military problems lies in the area of tactical communications. An important requirement for such systems is the capability to be rapidly deployed, reconfigured, and expanded. Experiments to test the ability of the system in such tasks should be made. Such experiments can be made by testing different configurations of the network dynamically as the configuration is changed. For example, the network can be set up to cover some area with a hole in the middle and then expanded to fill the hole. If users are using the network, or if users are simulated while the network is being reconfigured, the dynamics of the deployment can be explored. Other experiments involving dynamic reallocation of communications capacity and network vulnerability to the failure of repeaters and stations should also be supported by the experimental system.

7.3.3 Mixes of Users

Most military tactical networks and systems must support a mixture of users. Slow-speed general-purpose terminals, higher speed special-purpose terminals, very slow sensors, and very high-speed file-transfer terminals (such as mini-computers) may all require access to the same network. Terminal characteristics may also vary in that different length packets will be sent by the different terminals. It will be important to understand the interaction of mixes of terminals to apply the PR concept to military problems.

The experimental system should be designed to support a wide variety of terminals, and so that terminal parameters can be easily and rapidly varied.

7.4 PARAMETERS TO BE MEASURED

7.4.1 Link Parameters

The following link parameters should be measured:

a. Bit error rate
b. Propagation statistics
c. Noise statistics
d. Bit error patterns
e. Co-user parameters (time, frequency, and power statistics)
f. Retransmission rate
g. Channel Utilization
h. Signal/noise and signal/interference ratio prior to detector.

7.4.2 Network Parameters

The following network parameters should be measured:

a. Throughput (see paragraph 7.2.2.a for definition)
b. Delay (see paragraph 7.2.2.b for definition)
c. Blocking (see paragraph 7.2.2.c for definition)
d. Loss (see paragraph 7.2.2.c for definition).

7.4.3 Station Parameters

The following station parameters should be measured:

a. Rate of IP's offered to terminals
b. Number of IP's Echo Ack
c. Number of IP's ETE Ack
d. Number of distinct IP's received from terminals
e. Total number of IP's received from terminals. When a second copy of an IP is received, it is necessary to determine whether the packet was reactivated or was a retransmission from a device that did not receive an Echo Ack. This can be done by comparing the times of the arrivals of the two packets.

NOTE

Measurements b. through e. should be recorded as a function of time.

f. Average number of retransmissions
g. Average number of reactivations
h. Number of IP's dropped after maximum number of reactivations
i. Channel traffic at station
j. Occupancy of various parts of storage at the station.
k. Fraction of various types of packets transmitted by station (e.g., IP's, RSP's ETE Ack's, and control packets)
l. Time delay to complete the process of repeater initialization, labeling, and testing of repeater-station network.
m. Average time delay from first transmission of an IP until receiving an ETE Ack from the terminal
n. Utilization of control processing unit (cpu).

7.4.4 Terminal Parameters

a. Rate of IP's offered to terminals
b. Number of IP's Echo Ack
c. Number of IP's ETE Ack
d. Number of distinct IP's received from terminals
e. Total number of IP's received from terminals. When a second copy of an IP is received, it is necessary to determine whether the packet was reactivated or was a retransmission from a device that did not receive an Echo Ack. This can be done by comparing the times of the arrivals of the two packets.
f. Average number of retransmissions
g. Average number of reactivations
h. Number of IP's dropped after maximum number of reactivations
i. Time delay to identify specific repeater
j. Time delay to establish communication with a station
k. Time delay for receiving ETE Ack from station to an IP
l. Terminal interaction delay as a function of the number of IP's
m. Number of terminals blocked.
n. Number of IP's lost when terminal departs from system.

7.4.5 Repeater Parameters

a. Occupancy of buffers (packets stored for transmission TO station and FROM station)
b. Number of packets successfully repeated (received Echo Ack) TO and FROM station
c. Number of packets dropped after MNT
d. Number of times search procedure used, or number of times addressed packet to ALL. This depends on the particular routing scheme.
e. Average number of retransmissions.

7.5 FACILITIES

7.5.1 Link Measurements

Facilities required to support the link measurements are:

a. Three repeaters including rf and logic. One repeater should be interfaced to the minicomputer in the propagation and noise measurement van. Two repeaters should be interfaced to packet terminal simulators so that it can operate as a terminal, as a repeater, or as an artificial traffic source.
b. The existing rf measurement facility housed in a mobile van.
c. A test area with coexisting users in the band.

7.5.2 Network Measurements

Facilities required to support the network measurements are:

a. Thirteen repeaters including rf and logic. All should be capable of operating as stand-alone repeaters, two should be interfaced to minicomputers to operate as a station and a simulated station, and six should be interfaced to terminals or terminal simulators.
b. A station.
c. A station simulator.
d. Six terminals or terminal simulators (at least two of these must be capable of generating artificial traffic).

7.5.3 Facilities for User Experiments

The following facilities are needed for user measurements:

a. Seven repeaters operating as such.
b. One station.
c. Fourteen terminals.
d. Two artificial traffic sources.
e. A repeater rf and logic interfaced to a minicomputer to operate either as a high-speed traffic source or as a simulated station.

8.1 INTRODUCTION

This subsection of the system plan addresses the first prototype equipments planned for packet radio experiments. The material is intended to satisfy the following needs of the continuing experimental process:

a. To identify and describe the equipment capability required for the initial system experiments.

b. To provide a baseline and direction for the design, layout, fabrication, assembly, and checkout of these prototype equipments.

c. To provide projected performance parameters for use in network modeling and system evaluations.

The three network elements (repeater, terminal, station) are defined in paragraph 8.2. The elements are partitioned into basic functional areas and the primary interfaces are identified and discussed.

Paragraphs 8.3 through 8.5 expand and provide further detail on each of these basic functional areas. A family of functional elements are described that can be assembled in different configurations to satisfy the needs of the three types of network elements.

Paragraph 8.6 through 8.9 address the prototype repeater, terminal, and station, respectively. The functional elements defined in the preceding sections are grouped to form the prototype equipments. The composite characteristics of each equipment are summarized and the packaging and power supply factors are discussed.

The discussion of the prototype station does not cover the station processor. This material will be included in the design plan as the investigations in that area progress.

8.1.1 Mission of the Prototype Equipments

The packet radio project goals are presented in section 2 along with a series of experimental objectives. The prototype equipments characterized in this section of the plan represent a first step in this experimental process. The mission defined for the initial prototype equipments is:

a. To provide a research capability with several degrees of freedom with which specific communication link and basic network experiments can be accomplished.

b. To serve as a focus for the development and testing of promising new technology.

c. To provide a flexible research vehicle that is open-ended in the sense that more sophisticated techniques (for example, larger spreads, multiple channels, or frequency hopping) can be added as the experiments progress.

These initial prototype network elements are prerequisites for the experimental process. As the experiments progress, the mission and the characteristics of the network elements can be expected to change.

8.1.2 Design Guidelines

In accordance with the established mission, the following guidelines are established for the design of the prototype equipments.

a. Modularity. The prototype equipments will be organized and constructed as a set of functional modules. This is to facilitate the modification and/or change of specific features as the system design matures. Functional boundaries and defined interfaces will be established and will be adhered to strictly.

b. Size and Weight. Repeaters are ruggedized, man-transportable units. Terminals are also man-transportable with the capability of being reduced to hand-held size. The initial equipments will be as compact as possible, using available components and construction techniques. The goal of small, compact equipments must be balanced against the requirements imposed by the experimental mission of the equipments (i.e., including option features, provisions for modification and change).

c. Low Power. Power drain is a very critical factor. Every effort will be made to reduce the power drain and extend battery life. Low power circuit techniques and devices are to be used and functions turned off during periods where they are not needed.

d. Cost. The ultimate cost of repeater and terminals will have an important bearing on the success of the distributed radio network concept. An effort will be directed at techniques for reducing the cost associated with the composite network elements. The main thrust in this area will be directed at finding new ways of achieving the classical radio and signal processing functions and not at just cost reduction per se.

e. Reliability. The prototype elements will be used to execute a series of experiments. The operation of these elements must be consistent and repeatable so as not to mask or degrade the experimental data. Also, the equipments must be available and operational for a large percentage of the time so that the experiments can proceed as scheduled. Quality components and construction techniques coupled with well-conceived and tested designs are needed. Maintenance features, including monitoring and self-test, must be considered during the design cycle and provided as an integrated part of each prototype equipment.

8.2 FUNCTIONAL DEFINITION

The functional definition provides insight into the general functions of the network elements. It also defines the primary interfaces within each network element and includes specific information concerning electrical, physical and operational parameters.

8.2.1 General Network Description

The packet radio network consists of three network elements. These are stations, repeaters and terminals (figure 8.2-1). Brief functional descriptions of these elements in their prototype form for the experimental system are contained in the next three sections.

8.2.2 Functional Description

8.2.2.1 Prototype Station

A station is the interface element between the packet radio network and the ARPANET. The station has a broadcast access to the other elements in the PRN; i.e., repeaters and terminals. This access in its minimum form will be identical to the prototype repeater. The station performs packet buffering, accounting, directing and routing, and monitoring/control for the network of associated repeaters and terminals.

8.2.2.2 Prototype Repeater

The sole function of the repeater element is to extend the effective range of terminal-station links. The repeater, therefore, performs one basic function of receiving and transmitting packets in the network. The repeater has access to the broadcast channel to receive and transmit packets. It additionally has the function of detecting errors in packets, as well as routing packets under the direction of the station element.

8.2.2.3 Prototype Terminal

The prototype terminal is the interface element between the user and the packet radio network. It provides the interface to user I/O devices, such as, teletype, crt display, and minicomputer. The terminal element buffers and formats packets for entry into the packet radio network.

8.2.3 Interface Definitions

The interface definitions are based on primary boundaries dictated by the multiple application of radio and digital equipments in the station, repeater and terminal. The four primary boundaries are rf/channel interface, modem/digital interface, station/processor interface, terminal I/O device interface.

8.2.3.1 RF/Channel Interface

The rf channel interface is defined via three categories which are electrical, physical, and operational parameters.

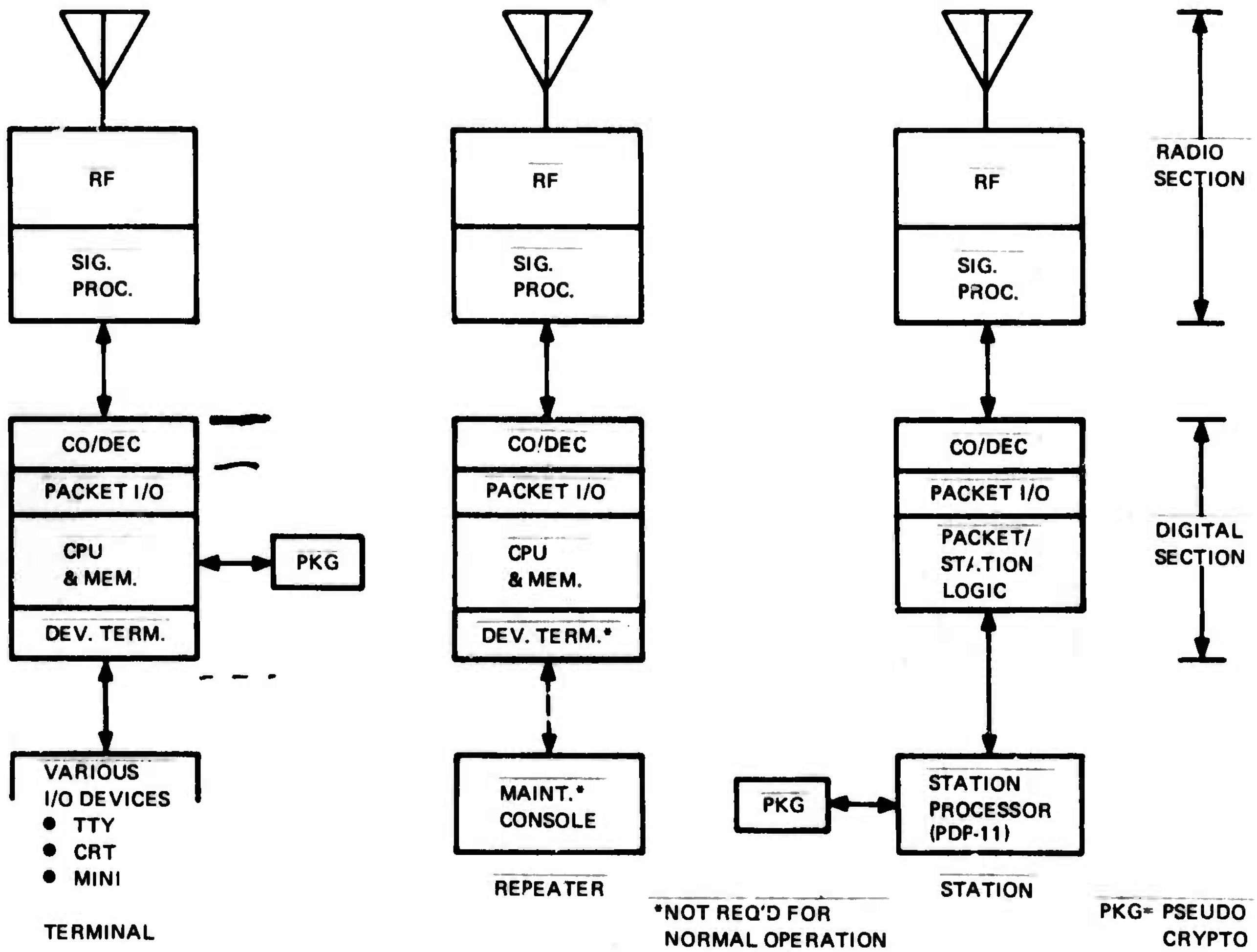


Figure 8.2-1. Functional Diagram - Prototype Equipments.

a. Electrical Parameters. The electrical parameters of both transmit and receive are as follows:

1. Receive and Transmit Frequency Band. 1- to 2-GHz with target band 1.71 to 1.85 GHz selectable channel spacing with 12.6-MHz channel spacing. The occupied channel bandwidth is 20 MHz.

2. Receive Signal Level. -100 dBm to 0 dBm.

3. Transmit Signal Level. Repeater and station 49 dBm ERP (Effective Radiated Power)

4. Terminal. 40 dBm ERP

5. Physical Parameters. Repeater and station antenna is a minimum height of 45m with terminal antenna height at 3m. The maximum range between repeater-repeater and repeater-station links is 32 miles (radio horizon). The maximum range for repeater-terminal links is 1.4 miles.

b. Operational Parameters. The transmit-receive operation for all three network prototype elements is half duplex. The channel access for packet transmission has two modes (random access (ALOHA) and packet coherent carrier sense.

The transmitter's effective radiated power is controllable over 20-dB dynamic range in four steps. The occupied bandwidth remains constant for either high or low data rate by varying the code spread.

8.2.3.2 Modem/Digital Interface

The interface between the signal processing and detection circuitry and the digital interface gateway to the microprocessor is made up of 17 control lines. These control lines can be functionally divided into transmit, receive, and frequency control and masterclock segments.

a. Electrical Parameters. The interface circuitry is assumed to be C-MOS with all mnemonics that are true are equal to #5 volts. Signal absence equals 0 volt.

b. Physical Parameters. It is assumed that modem and digital sections are colocated. Line drivers would be required for any other configuration.

c. Operational Parameters. The operational description of the interface is divided functionally into transmit, receive, and frequency control and master clocks segments.

1. Transmit.

(a) TX Hi/Lo Rate. From digital to modem, identifies high or low data rate. High rate is ±5V and 0V is low data rate. It precedes all other transmit control interface transitions from digital section to modem.

(b) Carrier Sense. From modem to digital, when there is detection of packet transmission, line is +5V; otherwise, 0V. This is used to inhibit transmitting packets when in the carrier sense access mode.

Rec

(c) TX Enable. From digital to modem, disables receiver functions and turns on transmitter PA and preamble/encoder circuitry for duration of packet. The 0V transition means end of data transfer. Modulator must store bits and continue to transmit until bit storage is exhausted.

(d) TX EOP (End of Preamble). Modem to digital, after TX Enab (c.) transition and preamble sequence (generated internally in modem) is transmitted, TX EOP asks for bit data to be transmitted. Logic transition occurs synchronously with selected (Hi/Lo) master clock.

(e) TX Data. Digital to modem, bit data to be transmitted in NRZ format. Data transitions coincide with positive edge of selected (Hi/Lo) master clock.

(f) TX Power Control. Digital to modem, two lines that control power output of transmitter PA lines must be stabilized before TX Enab (c.) and during packet transmission interval. This provides four levels of power control.

(g)

2. Receive.

TR Clock

(a) RCV Enable. Digital to modem, activates receiver functions in modem (search for preamble, agc, and data detection functions). Remains in enable mode until packet is received.

(b) RCV Packet Sync. Modem to digital, signals the receipt of packet and end of preamble. Positive transition coincides with first received data bit. RCV packet sync is reset when RCV enable (g.) is reset.

(c) RCV Data. Modem to digital, synchronous with receive bit clock and in NRZ format.

(d) RCV Data Clock. Modem to digital, same as master clock with phase arbitrary, high and low rate on same line. The phase changes only during time between RCV Enable (g.) and RCV packet sync (h.). Clock stable all other times.

3. Master Clocks and Frequency Control.

Master Clocks. Modem to digital, two lines for free running 100 and 420 kBps clocks with stability of ±1 ppm.

Frequency Control. Digital to modem, four lines for control of digital frequency synthesizer.

8.2.3.4 Terminal I/O Device Interface

This interface is between the terminal microprocessor and the various I/O devices (tty, crt).

a. Electrical Parameters. Circuitry on both sides of this interface is COS-MOS. All mnemonics that are true are at +5V level with false defined as 0V.

b. Physical Parameters. The terminal and I/O devices are assumed to be colocated. If not, line drivers/terminators will be necessary for other configurations.

c. Operational Parameters. The interface between processor and one I/O device consists of 21 lines of which 16 are the 16-bit parallel data bus. They are the following:

Data Bus	The 16-bit bi-directional tri-state data bus for transferring data to/from the processor or I/O device.
Interrupt Request	From I/O to processor line that signals the processor that the I/O device needs servicing.
Interrupt Select Status	The processor control flag used to identify the interrupting device. This signal causes any device that has raised the interrupt line (may be more than one) to respond with a bit on the data bus. The data bit is correlated by the program to a Device Address.
Decoded Address	A unique address line that specifies a particular I/O device.
Read Peripheral (RDP)	The processor control flag that reads data from the bus into the processor. This flag also causes the tri-state latch in the I/O device to put data on the bus.
Write Peripheral (WRP)	The processor control flag that causes data from the processor to be put on the data bus. This flag also strobes data into the I/O device input latch.

Reading into the microprocessor requires that the interrupt request be activated for each 16-bit parallel word. For more detailed information, refer to paragraph 8.4.6.1 and figure 8.4-18.

8.2.3.3 Station Processor Interface

This is the interface between the microprocessor and the station processor which is assumed to be a minicomputer.

a. Electrical Parameters. Circuitry on both sides of interface is COS-MOS. All mnemonics that are true are at +5V with absence of mnemonic being 0V.

b. Physical Parameters. The microprocessor and station processor are colocated and, therefore, should not require line driver/terminators.

c. Operational Parameters. The interface consists of a direct memory access channel and necessary interrupt and control flags for block transfer directly into the microprocessor memory. The interface lines are the following:

Data Bus	The 16-bit bi-directional data bus that transfers data to/from the microprocessor.
Address Bus	The 16-bit bus used for access to memory.
Interrupt Request	The signal to the microprocessor that the station needs service. A separate level of interrupt is defined for this application that allows the microprocessor to identify the station.
Read Peripheral (RDP)	The processor control flag that takes data into the processor. This flag along with an address causes a specific device to put data on the data bus.
Write Peripheral (WRP)	The processor control flag that signals that data from the processor is on the data bus. This flag, along with an address causes a specific device to take data from the data bus.
Halt	Used as an interrupt to the station processor. Indicates DMA (direct memory access) initialization has been completed and data transfer can start. Microprocessor will not start until the block data transfer is complete.
Start	Signals microprocessor the data transfer is complete. Restarts microprocessor.
Memory Enable	Signal that allows access to the microprocessor memory used along with an address on the address bus. This signal contains the memory access timing.
Memory Read/Write	Signal which defines the memory data transfer as to or from memory.

For more detailed information, refer to paragraph 8.4.6.2 and figure 8.4-19.

8.3 RADIO PLAN

This subsection of the equipment design plan for the ARPA experimental packet radio network is concerned with the radio. The radio section includes not only the rf head and antenna, but also includes rf conversion stages and signal processing, both in transmitted digital-to-analog conversion processes and receiver analog-to-digital detection processes.

The radio plan includes two major sections: a general description and a detail design section. The general description section includes an overview of the radio with an operational description of the radio major functions and a performance specification summary. The design details offer a radio design plan that meets the performance objectives stated in section 5. The results of this design detail are discussed in paragraph 8.3.2, Performance Specification Summary.

8.3.1 General Description

The general description for the radio includes four major sections. Each section addresses major design objectives.

8.3.1.1 Modulation

The basic mode of modulation for digital communication for the packet radio network is spread spectrum form by means of pseudonoise (PN) code spreading. PN code spread spectrum is used to reduce rf interference to packet radio non-users by virtue of less watts/Hz radiated in a given band. Also, reception is enhanced in the presence of undesired narrowband interferers.

The design modulation for chip modulation is minimum shift keying (msk) with an effective bandwidth of approximately 20 MHz (first nulls in the msk spectrum).

Bit modulation is differentially coherent and was chosen because of the following. Since surface acoustic wave device (SAWD) matched filters are used for efficient data correlation, the requirements for coherent detection (and attendant equipment complexities) is not required. Differentially coherent detection is approximately as good, performance-wise, as coherent modulation for the E_b/N_o expected. (See appendix C.1 for discussion of this parameter.) Differential detection requires phase coherence only at the SAWD interfaces. Envelope detection is performed at the differential SAWD outputs.

Code spread is generated by discrete (digital) circuits operating at the chip rate modulating a matched filter of two chip length impulse response. Data bit determines whether code or code inverted (chip value inverted) is generated for transmission.

Two data rates are used, one high rate and one low rate. Constant chip rate is used in both rates, which means the spread factor differs for the two rates. Low rate (100 kBps) is used for terminal-to-repeater where severe multipath and fading phenomena is anticipated. The spread factor is 126. Repeater-to-repeater traffic is line-of-sight to the horizon (if repeaters are properly placed), so higher bit rates (420 kBps) and

lower spread factors (30) may be sustained without radio performance degradation.

This higher rate between repeaters should improve packet throughput since repeaters are transparent to terminal and station, and higher rates mean shorter packet duration intervals.

8.3.1.2 Preamble Organization

The preamble (does not include header of text) is organized to perform three basic functions in the receiver:

a. Automatic gain control (agc) for receiver amplifiers to normalize rf signal levels to signal processing and detection circuits

b. Bit rate acquisition and synchronization

c. End of preamble (EOP) detection and start of text data to the microprocessor

A total of 39 bits of preamble are used. Appendix C.2 discusses in detail the requirements for bit length versus E_b/N_o ratio for given probability of miss and probability of false alarm. The method chosen (described in the detail design section) was based primarily on ease of implementation and lowest power consumption, rather than on shortest possible preamble.

The last 26 bits are used for EOP detection. Coherent agc requires several bits for operation, for which 13 are allowed before EOP detection starts. Bit sync acquisition is allowed for the total 39 bits since EOP is asynchronous detection. Bit sync is achieved by conventional phase-lock loop techniques. Digital phase-lock loops and also digital filter averaging are being investigated for possible uses in bit sync acquisition. Preamble is generated by three 13-bit Barker sequences, transmitted sequentially by Barker, $\overline{\text{Barker}}$, Barker, for 39 bits total.

8.3.1.3 Transmitter

The transmitter (and receiver) is functionally shown in figure 8.3-1. The transmitter functions include the encoder/modulator, up-conversion, power amplifier, terminal/repeater (T/R) switch and the antenna. The T/R switch and the antenna are time-shared with the receiver, as is the frequency generation equipment and control/monitor logic.

The primary functions of the transmitter are to accept data packets (including header) from the microprocessor, generate a preamble prefixing the packet, chip encode the total packet with the spread spectrum code, convert this digital signal to msk, up-convert to rf output frequency, amplify this up-converted signal to 10 watts maximum (also power control to set output power), filter, and radiate to the rf media through the antenna.

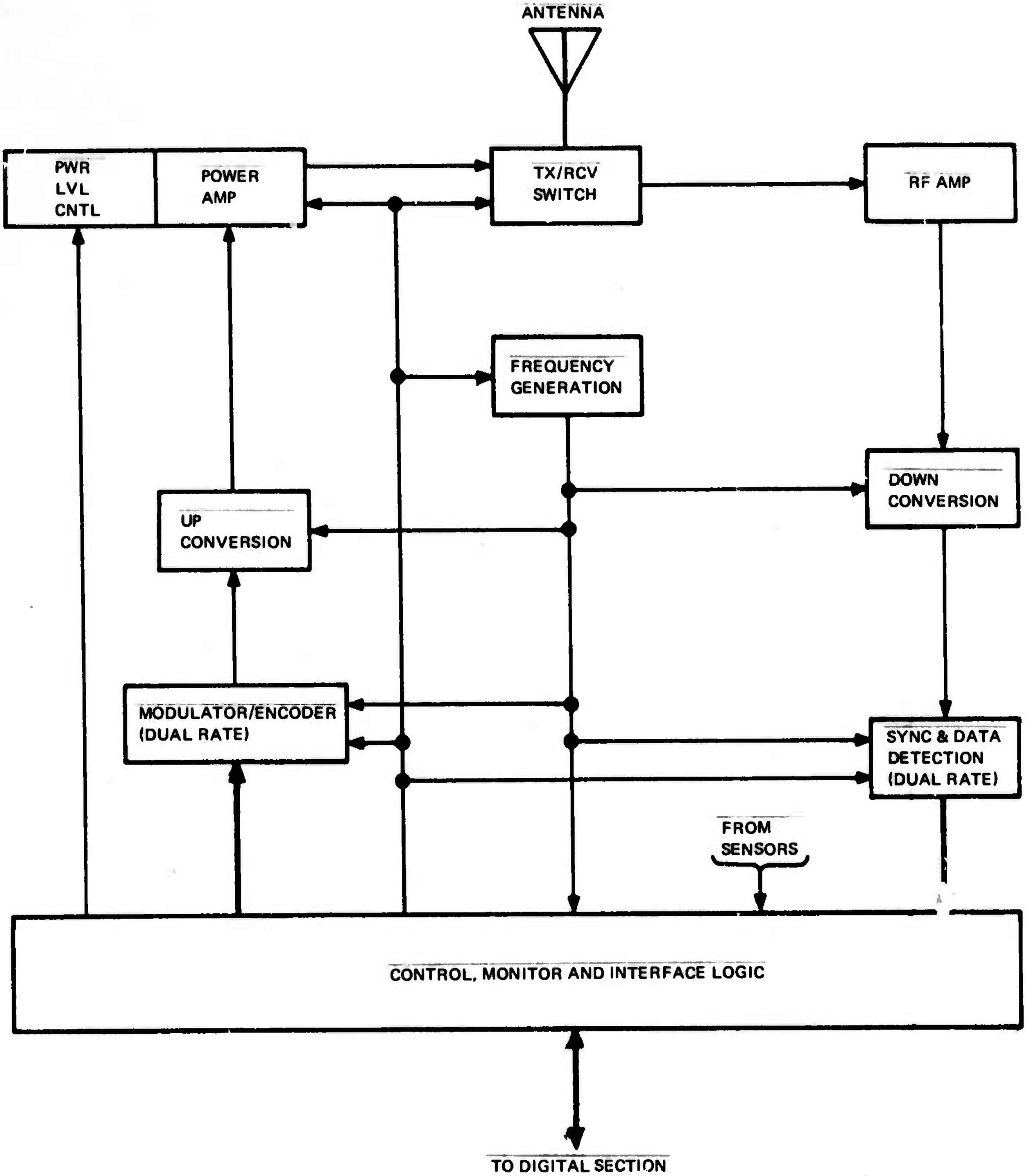


Figure 8.3-1. Radio Section Functional Diagram.

8.3.1.4 Receiver

The primary functions of the receiver operations (not including T/R switching and frequency generation) are rf preamplification, down-conversion, signal gain control (includes both noncoherent and coherent agc), matched filter signal detection (SAWDs), preamble detection and bit sync acquisition, and data detection.

Common matched filters are used for preamble and data. This reduces complexities of receiver, but still retains performance objectives.

Dual rate detection is accomplished by using independent signal processing circuits for each rate. Low rate (100 kBps) is intended for terminal/repeater traffic, while high rate (420 kBps) is used for repeater/repeater traffic. Repeater/repeater traffic is line-of-sight, so multipath effects and fading are negligible and therefore, high data rates may be sustained over these links. Note that terminal equipment does not require high rate signal processing.

Multiple detector signal processing is identical to single detectors in implementation. Of course, additional modules are required for each multiple detector. Multiple detectors have the inherent problem of acquiring packets in the presence of other packets. This time discrimination is accomplished by generating a blanking signal from the first signal processing detector. This blanking signal disables the succeeding multiple detectors from acquiring packets in that time interval.

The following assumptions must be made to allow multiple detectors to operate properly:

a. Packets may overlap in time, but must not overlap preambles.

b. Bit timing (matched filter correlation peaks) of multiple packets must not coincide during the blanking interval.

c. Composite receive signal levels to individual packet signal level must be within 10 dB of each other to overcome matched filter processing gain and E_b/N_o requirements.

8.3.1.5 Frequency Generation

The frequency generation plan basically generates two types of signals. One is local oscillator (LO) frequency generation for up-/down-converter use. The other is various stable clock rates for chip and bit timing.

If SAWDs are of sufficient accuracy, one frequency standard is required for both frequency generation requirements. However, since SAWDs cannot be built to absolute frequency requirements in the time frame for the experimental packet radio initial development, SAWDs can be built that frequency match each other (±2 kHz) within an absolute frequency of ±20 kHz of the desired if. The LO frequency is adjusted to set the output/input frequency at the antenna to an absolute frequency.

The LO generation is thus completely separate from the chip/bit frequency generation, each with a stable frequency standard. When SAWD technology progresses to where absolute frequency requirements are feasible, one frequency standard may be eliminated from the frequency generation equipment.

8.3.2 Performance Specification Summary for Radio Plan

Frequency Band	~~Approximately 150-MHz bandwidth in 1000 to 2000 MHz range~~
	1710 to 1850 MHz primary target band
Frequency Channel Spacing	12.8 MHz
Transmitter Power Output	10 watts maximum into antenna
	20-dB power control in four steps 100 mW = 2 mi.
Transmitter Spurious Output	≥ 50 dB below ~~desired output~~ low in-band, 20-MHz bandwidth
Antenna	Colinear array (three elements) with 9 dBi gain (repeater)
	0 dBi gain (terminal)
Modulation	~~Pseudonoise~~ Code spread spectrum 127
Chip Modulation	MSK (minimum shift keying)
Occupied Bandwidth	20 MHz for 95-percent transmitted energy
Bit Modulation	Differentially coherent
Chip Rate	12.6 megachip per second (MCps)
Bit Rates (Dual) 25 k	100 kBps at lo rate — terminal/repeater traffic SF=128
100	400 kBps at hi rate — repeater/repeater traffic SF=32
SAW Receiver Processing Gain	+21 dB @ 100 kb 15 dB @ 400 kb
Receiver Signal Level	-100 dBm to 0 dBm (linear to -20 dBm) linear receiver
	Min usable signal at antenna
Noise Figure	≤ 10 dB 3 dB in preamp / 6 in filter, get 2 poles at once
Receiver Noise Bandwidth	20-MHz determined by if. 5-pole Butterworth filter IF etc

Preamp to get better noise fig

.5 V

Interference Levels	In-band interferers (±10 MHz of carrier)/ Signal: $\leq$ 10 dB above signal in linear range of receiver
Receiver Spurious Rejection	
Intermodulation and spurious components:	$\geq$ 60 dB in any 20-MHz bandwidth including processing gain
Transmit/Receive Filter:	5-pole Chebyshev filter, BW = 140 MHz
Image Rejection:	$\geq$ 80 dB
Access	Random access (nonslotted ALOHA) Coherent carrier sense (threshold set at -103 dBm)
Range	Terminal/Repeater: 1.4 mile for 99-percent of detection in an urban environment Repeater/Repeater: Line-of-sight for up to 32 miles (radio horizon)
BER Performance	$Pe \leq 10^{-5}$
Pseudonoise Spread Factors	126 chips/bit at Lo rate 30 chips/bit at Hi rate
Coding	63 chips/subchannel at Lo rate 15 chips/subchannel at Hi rate
Preamble	Length: 39 bits 13-bit Barker code 13-bit inverted Barker code followed by 13-bit Barker code Probability of Detection: (0.999 design goal) Probability of False Alarm: 10^{-6}

8.3.3 Modem/Digital Interface

TX ENABLE

TX HI/LO DATA RATE

TX END OF PREAMBLE

TX DATA

TX POWER CONTROL (2 bits)

RCV ENABLE

RCV END OF PREAMBLE

RCV DATA

RCV BIT CLOCK

MASTER CLOCKS (100 and 420 kBps)

CARRIER SENSE, COHERENT

FREQUENCY CONTROL (4 bits)

STATUS & MONITOR

8.3.4 Design Details

Each of the functional elements comprising the radio is discussed in further detail in this subsection of the report. In each, the functional element is briefly described and its interface defined. A performance and function analysis follow. Data, such as power dissipation and physical characteristics, are included for each functional element.

8.3.4.1 Encoder/Modulator

a. Functional Description. The encoder accepts packet data from the microprocessor interface, inserts a preamble code, and chip codes the packet for code spread spectrum. The modulator accepts in chip form (digital) the coded packet and msk modulates at the radio if. carrier. Refer to Appendix C.6 for code selection criteria and the method to synthesize the actual code to be used.

b. Functional Interfaces

Tx Data	COS-MOS logic level data from microprocessor
Tx Enable	COS-MOS logic level from microprocessor that enables encoder/modulator functions
Hi/Lo Rate	COS-MOS logic level from microprocessor defining which data rate to transmit: 1 = Hi rate 0 = Lo rate
Clocks	${}_{L}R_{B}$ = Lo rate (100 kBps) bit clock, LP-TTL logic level ${}_{H}R_{B}$ = Hi rate (420 kBps) bit clock, LP-TTL logic level R_c = Chip clock (12.6 MCps) LP-TTL logic level
MSK Output	f_o ≈ 299.250 (±0.020) MHz (matched within ±0.002 MHz of receiver) P_o = 0 dBm, 50 ohms

c. Design and Performance Analysis. A functional block diagram of the dual rate encoder and modulator is shown in figure 8.3-2. The preamble is generated upon the receipt of a transmit enable pulse from the microprocessor. The preamble consists of 39 bits as shown in figure 8.3-3. The first 13 bits are for setting the agc level at the demodulator. The preamble for detecting the start of message consists of a 13-bit inverted Barker code followed by the 13-bit Barker code.

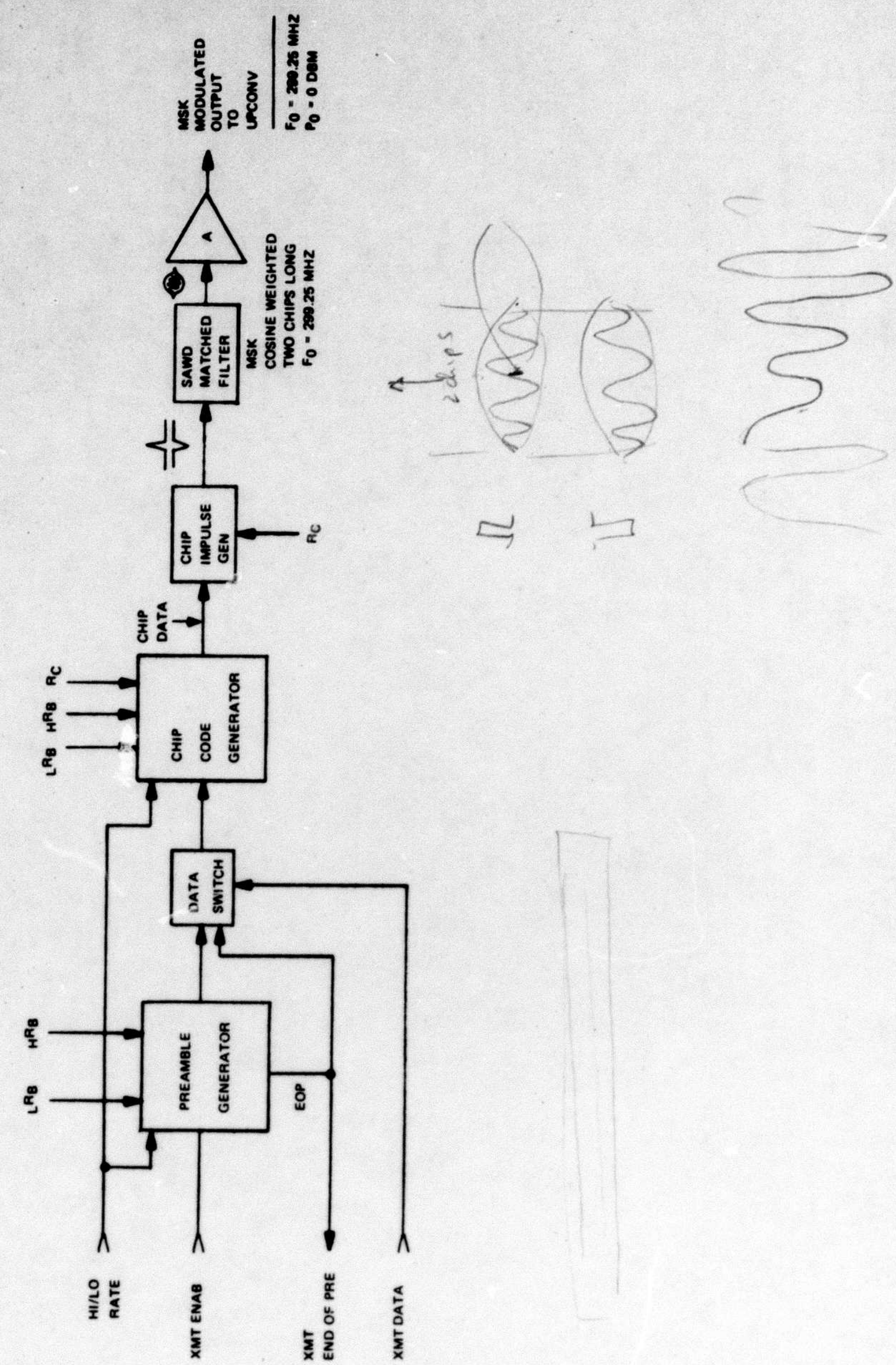


Figure 8.3-2. Encoder/Modulator (Dual Rate).

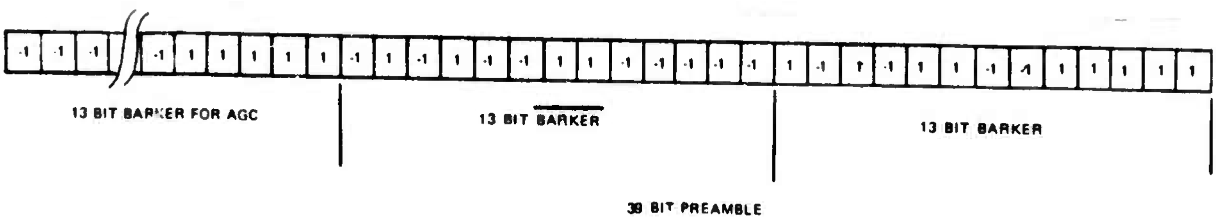


Figure 8.3-3. 39-Bit Preamble.

The preamble bits, as well as the subsequent data bits, are clocked at either the high rate of 420 kBps or low rate of 100 kBps. The preamble and data bits are differentially encoded by the algorithm

$$S_k = S_{k-1} \oplus d_k$$

where d_k is the k^{th} preamble or data bit, S_{k-1} is the $k-1^{th}$ encoder output bit, and S_k is the k^{th} encoder output bit. The symbol $\oplus$ indicates the exclusive-OR operator. A code generator generates chips at a 12.6 MCps rate. Thus, there are 126 chips per bit in the low rate mode and 30 chips per bit in the high rate mode. This is illustrated in figure 8.3-4. The chip code consists of two pseudo-orthogonal maximal length codes with one code being transmitted on each msk subcarrier. The chips at the output of the code generator alternate between one code and the other. In the low rate there are 63 chips/subchannel/bit, and in the high rate mode there are 15 chips/subchannel/bit. The chips are then exclusive-ORed with the preamble or data bits. Thus, in the low rate mode if the output at the bit encoder is a "0," the 126 chips are output to the chip impulse generator. If the output is a "1", each of the 126 chips from the code generator for that bit has its sign inverted. Therefore, in the low rate mode, the chip impulse generator sees two possible sequences of 126 chips. The difference between the sequences is that the signs of one are inverted relative to the other.

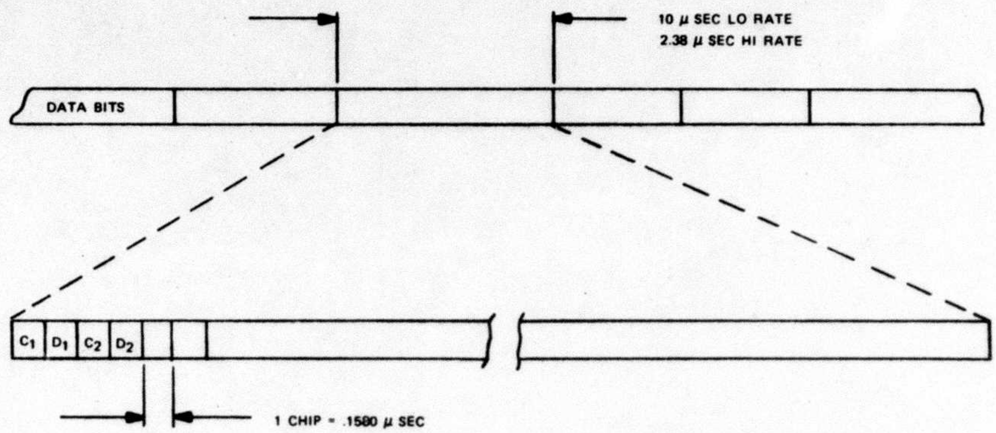


Figure 8.3-4. Code Spread Format.

The function of the chip impulse generator is to generate narrow bipolar impulses (5 to 10 ns) at a rate of 12.6×10^6 impulses/second that drive the SAWD. A "1" generates a positive impulse, a "0" generates a negative impulse. Minimum shift key (msk) modulation is used. An explanation of this modulation technique and its advantages is given in appendix C.1. The impulse response of the SAWD corresponds to a cosine weighted if. pulse of two chips in length of 0.159 μs. The SAWD is impulsed at the chip rate or every 0.0794 μs. To achieve the desired 90-degree phase shift of the msk subcarrier, generated by the first impulse relative to the subcarrier generated by the second impulse, requires that there be an odd number of half cycles of if. carrier in the two-chip interval. An if. frequency which satisfies this requirement is 299.25 MHz. The sequence of impulses at the chip rate yields the msk signal, which is then amplified and up-converted to the rf frequency.

d. Packaging Data. The preamble generator, code generator, and encoder are digital devices and may be constructed on printed circuit boards. The impulse generator, SAWDs, and rf amplifier should be in a shielded enclosure.

e. Control and Monitor. The control lines are defined in the functional interface. No monitor points are required.

f. Power Estimates.

	Power (mW)
Preamble Generator	20
Data Switch	1
Digital Encoder	20
Code Generator	300
Impulse Generator	100
SAWD	—
Amplifier	240
Total	680 mW

g. Additional Features. The encoder/modulator does not require high rate capability for the terminal. However, this cost is so slight that this feature will be in all encoders/modulators. Thus, the encoder/modulator will be identical and interchangeable for all terminal/repeater/station applications.

8.3.4.2 Up-Converter

a. Functional Description. The up-converter is functionally shown in figure 8.3-5. Its essential function is to convert the 299.25-MHz if. to the desired rf frequency range. This is accomplished by mixing the msk signal at if. frequency with a 1423.8- to 1537.2-MHz signal received from the local oscillator (LO) in a doubly balanced mixer. The resultant rf output from the mixer is bandpass filtered through a 140-MHz wide 2-pole Chebyshev filter centered at 1780 MHz. The filtered rf output is preamplified (gain = 7 dB) before it goes out of the up-converter to the power amplifier (PA).

b. Functional Interfaces.

IF Input	f_{IF} = 299.25-MHz msk signal
	BW = 20 MHz
	P_{IF} = 0(±3) dBm
LO Input	f_{LO} = 1423.8 to 1537.2 MHz
	P = +7(±3) dBm
RF Output (SSB)	f_o = 1723.05 to 1836.45 MHz
	P_o = 0 dBm minimum
	LO rejection ≥ 23 dB below desired output
	Lower sideband rejection ≥ 30 dB below desired output
	Spurious ≥ 50 dB below desired output

c. Design and Performance Analysis. In this section, it is shown that the if. frequency to the mixer has been selected such that the number of intermodulated spurious output frequencies close to the desired output rf frequency range is minimum. It is also shown that the power in the spurious frequencies is sufficiently suppressed due to the inherent IMP rejection capability of the mixer, combined with the attenuation characteristics of the 5-pole Chebyshev transmit/receive filter. A chart of sum mixing that plots f_o as a function of the f_L/f_H ratio and the percentage separation is provided for reference in figure 8.3-6. Of the two frequency inputs to the mixer, f_L is the lower and f_H is the higher frequency. In our case, f_L = 299.25 MHz and f_H refers to the LO frequency range from 1423.8 MHz to 1537.2 MHz. The 0-percent separation on the chart refers to the rf center frequency at the output of the mixer. In our case, this center frequency is 1780 MHz.

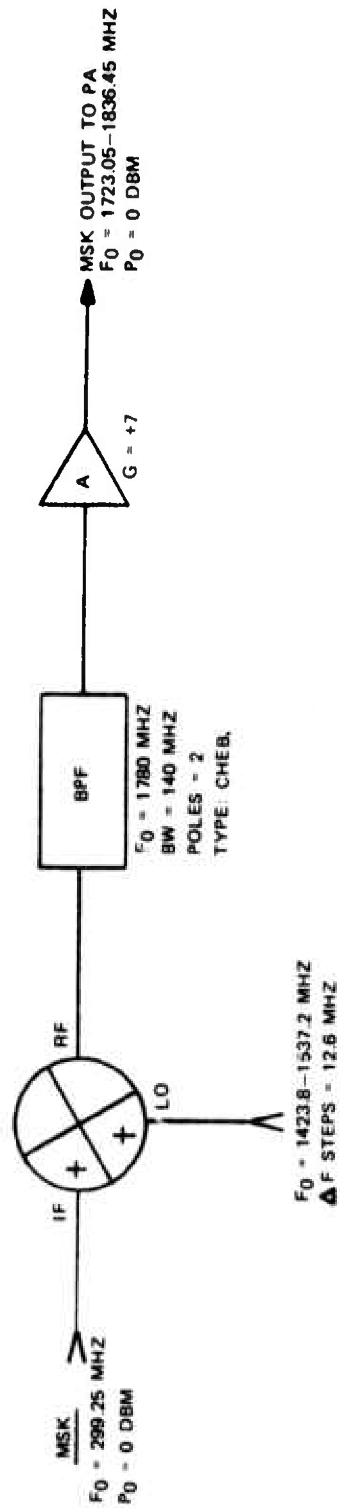


Figure 8.3-5. Up-Converter.

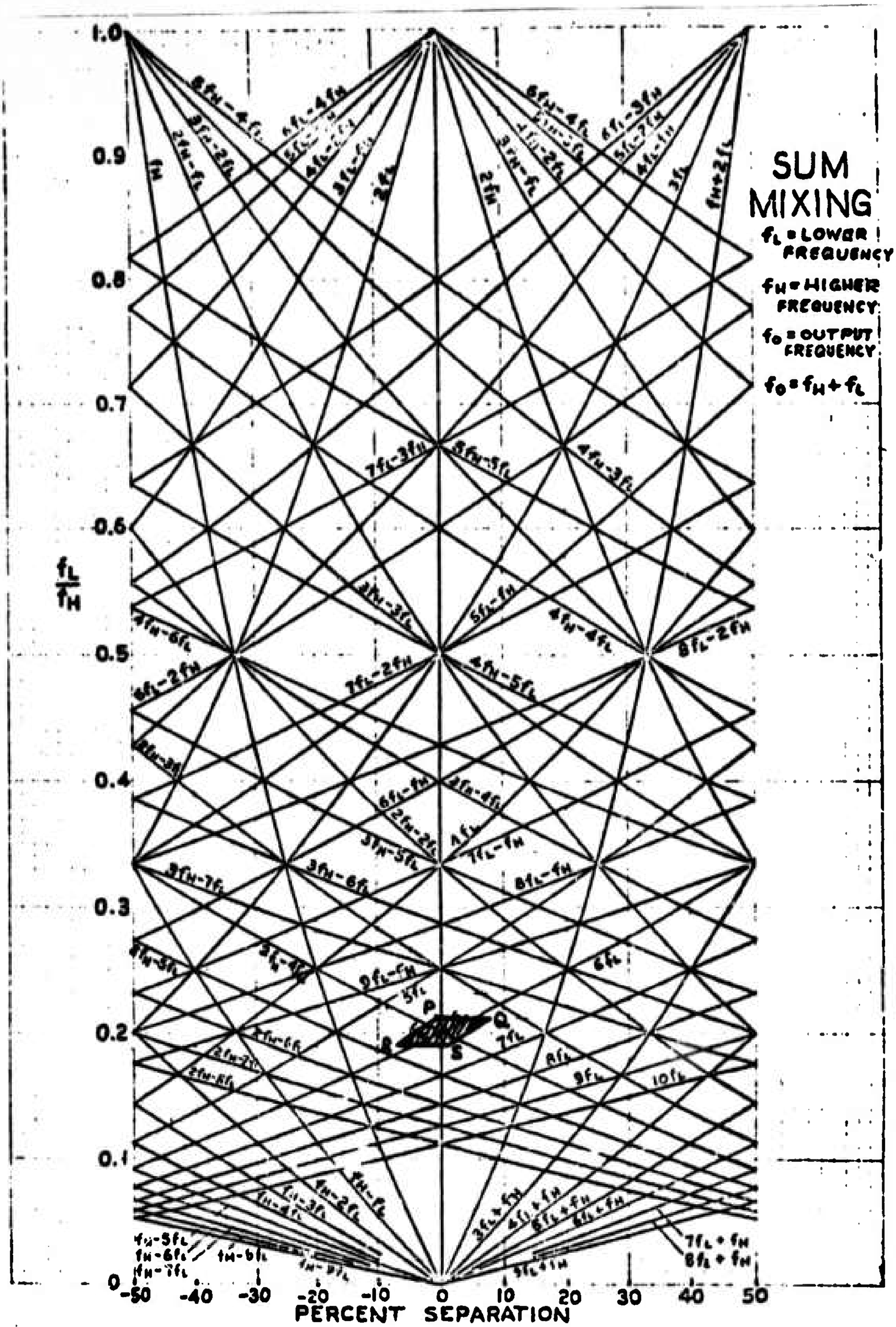


Figure 8.3-6. IMP Chart.

Corresponding to the highest LO frequency, f_L/f_H is 299.25/1537.2 = 0.19.
Corresponding to the lowest LO frequency, f_L/f_H is 299.25/1423.8 = 0.21.

The lowest LO frequency of 1423.8 MHz results in 1723.05-MHz frequency at the output of the mixer. The lower sideband frequency (3-dB point) of the bandpass filter is 1710 MHz, and the upper sideband frequency is 1850 MHz; 1710 MHz is -0.757 percent away from 1723.05 MHz, and 1850 MHz is +7.368 percent away from 1723.05 MHz. Hence, as shown in figure 8.3-6 and also in figure 8.3-7, we get the points P and Q, where P corresponds to a f_L/f_H = 0.21 ratio against -0.757-percent separation, and Q corresponds to a f_L/f_H = 0.21 ratio against +7.368-percent separation.

Now, the highest LO frequency of 1537.2 MHz results in 1836.45-MHz frequency at the output of the mixer. The lower sideband frequency of 1710 MHz is -6.886 percent away from 1836.45 MHz, and the upper sideband frequency of 1850 MHz is -0.738 percent away from 1836.45 MHz, thereby resulting in points R and S, respectively, on the above referenced figures. Points P, Q, R, and S form a trapezoid. It is clear from the referenced chart that intermodulation lines $6f_L$ and $2f_H-4f_L$ fall within this trapezoid. It is also obvious that as a worst-case condition, the effect of intermodulation frequencies $2f_H-3f_L$ and $2f_H-5f_L$ should also be considered. Intermodulation products of order 10 or greater are not analyzed since their IMP levels are sufficiently low.

Based on the above information, the power attenuation in each spurious frequency can be estimated up to the output of the 5-pole transmit filter. This estimate is provided in table 8.3-1. The data for the attenuation through filters is obtained from curves plotted in figure 8.3-8. The data for the IMP levels at the mixer output is based on some laboratory measurements obtained for a 1000- to 1400-MHz range mixer.

d. Packaging Data. The size of the up-converter is estimated to be 0.75 x 1 x 4 inches. Construction consists of microelectronic hybrid techniques in a shielded enclosure. Refer to paragraph 8.6 for integration into the mechanical rf assembly.

e. Control and Monitor. None

f. Power Estimate. 150 mW at +15 volts dc.

g. Additional Features. Up-converters for all network configurations (terminals/repeaters/stations) will be identical and interchangeable.

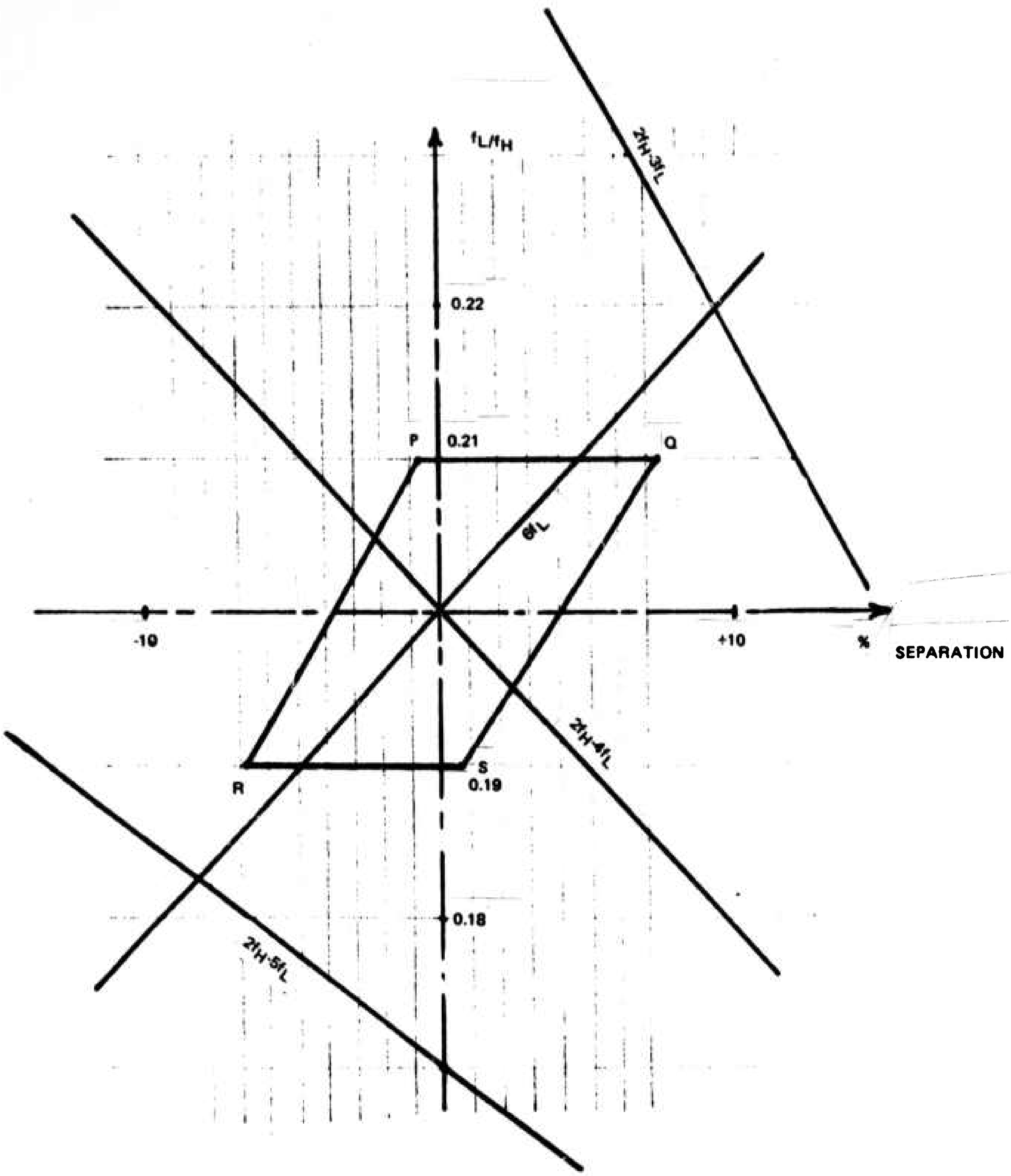


Figure 8.3-7. Expanded IMP Chart.

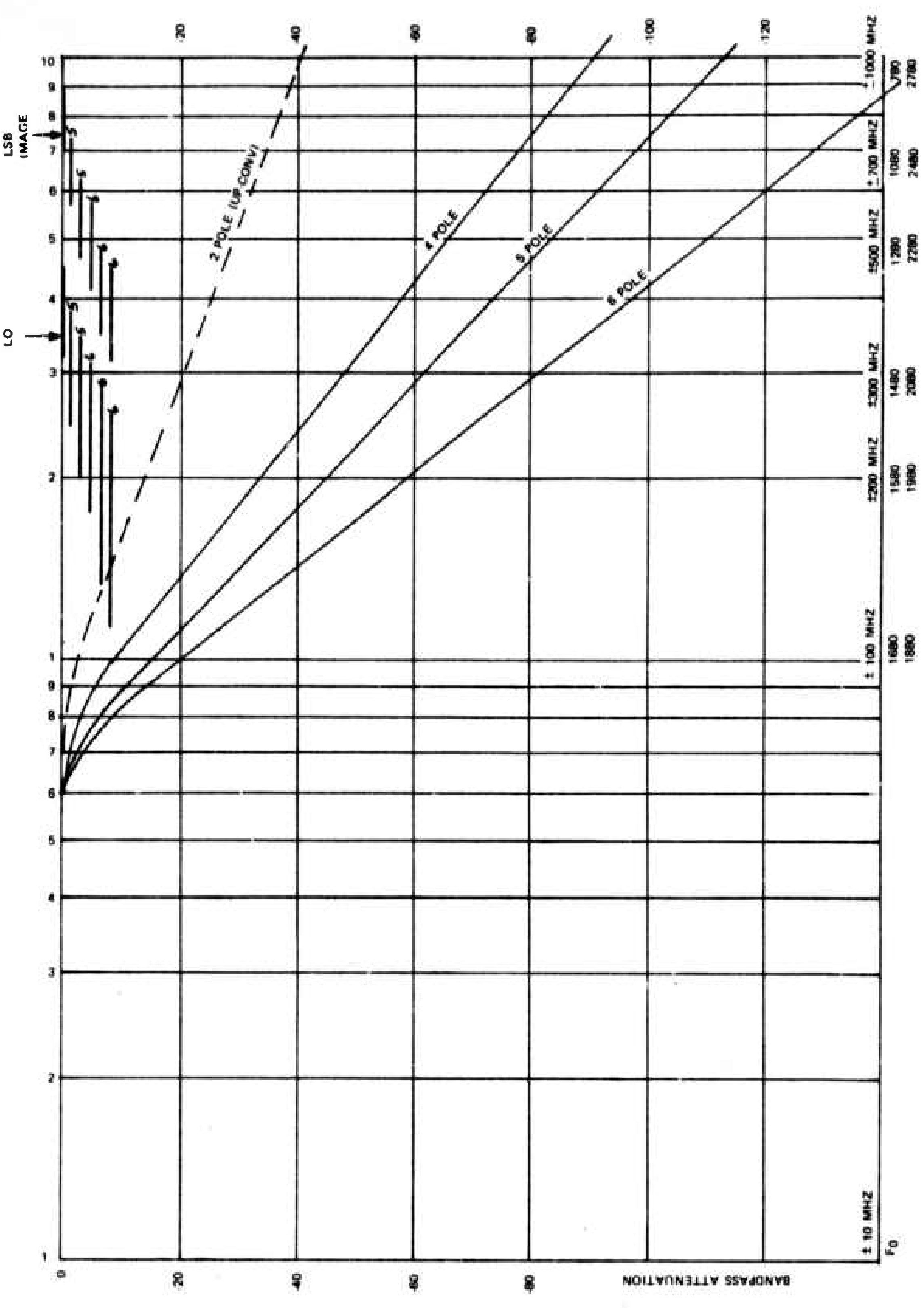


Figure 8.3-8. Bandpass Attenuation Through Filters.

Table 8.3-1. IMP Levels.

FREQUENCY (MHz)	IMP LEVEL* (dBm)	ATTENUATION (dB)		
		UP-CONVERTER FILTER (2-Pole Chebyshev)	TRANSMIT FILTER (5-Pole Chebyshev)	TOTAL
$f_H - f_L$ = 1124.55 to 1237.95	—	30-33	90-98	120-131
$2f_H - 4f_L$ = 1650.6 to 1877.4	-53	—	—	53
$6f_L$ = 1795.5	-58	—	—	58
$2f_H - 3f_L$ = 1949.85	-48	9	39	96
$2f_H - 5f_L$ = 1578.15	-48	14	47	109
f_L = 299.25	-20	Over 60	Over 60	Over 140
f_H = 1423.8 to 1537.2	-6	17-22	55-71	78-99

*Referenced to the desired output of the mixer with 0-dBm if. input.

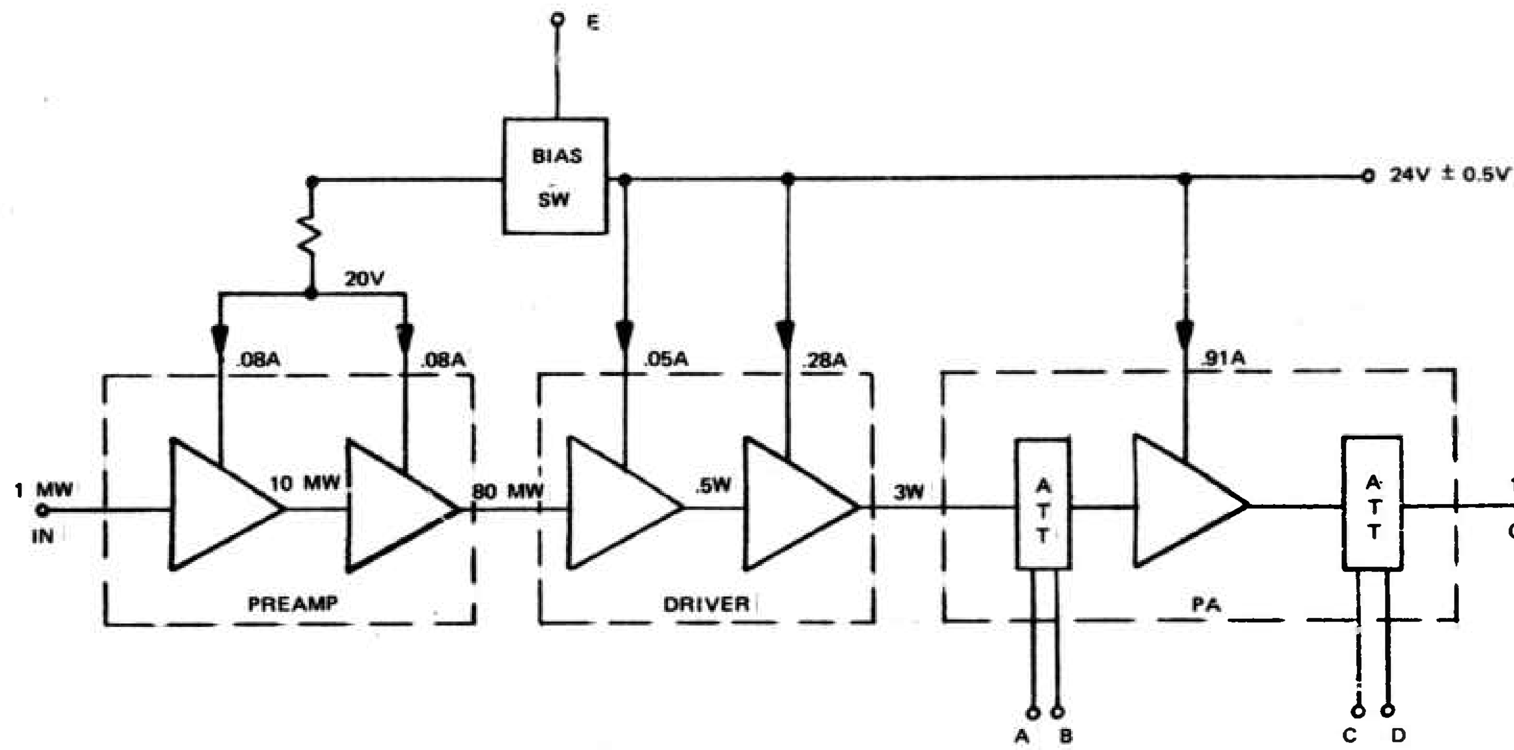
8.3.4.3 Power Amplifier and Power Control

a. Functional Description. Figure 8.3-9 details functional blocks of the PA. Power levels, etc., shown are assuming the worst-case frequency range of 1860 to 2000 MHz. A lower operating frequency will mean both higher power levels and higher gains available. The dashed lines indicate how the module might be broken up for testing/troubleshooting. Three subsystems make up the PA module:

1. Preamplifier
2. Driver
3. PA/power control circuit.

b. Functional Interface.

Frequency	Between 1 and 2 GHz (to be specified) (1.71- to 1.85-GHz target band)
Bandwidth	140 MHz
Gain	40 dB minimum
Output Power	12 W minimum (all operating extremes)
Input VSWR	2.5:1 maximum
Load VSWR	1.15:1 maximum
Input Power	1 mW minimum
Power Dissipation	Transmit 33 W cw operation, full power Receive 0.24 W
Supply Voltage	24 (±0.5) volts dc
Current Drain	Transmit 1.9 A (45 W) cw, full power Receive 0.01 A
Noise Output	-172 dBm/Hz (quiescent)
Power Control	20-dB minimum dynamic range of output control in four steps (step size to be determined)



OUTPUT	A	B	C	D
RATED	0V	0V	0V	0V
-1 STEP	5V	0V	0V	0V
-2 STEP	5V	5V	0V	0V
-3 STEP	5V	5V	5V	0V
-4 STEP	5V	5V	5V	5V

$$P_D = \underbrace{1.6 + 1.6}_{\text{PREAMP}} + \underbrace{1.3 + 6.7}_{\text{DRIVER}} + \underbrace{21.8}_{\text{PA}} + \underbrace{.001}_{\text{PIN}} \underbrace{-11.3}_{\text{POUT}} = 32.3W$$

η_c = 12 33 = 36.4%

I_T = 1.4A (EXCLUDING SWITCHES)

ALL LEVELS ASSUME CW OPERATION

Figure 8.3-9. Power Amplifier and Power Control.

Duty Cycle	Power Dissipation	Heat Sink
50%	22.5W	12 sq in. of 1 in. fins
25%	12.5W	6 sq in.
10%	4.5W	3 sq in.
5%	2.25W	case only

Power Control Lines

Output Power Control (in volts)

	A	B	C	D
Full Pwr	0	0	0	0
-5 dB	5	0	0	0
-10 dB	5	5	0	0
-15 dB	5	5	5	0
-20 dB	5	5	5	5

RF Connectors	SMA female
Weight	4 pounds maximum
Junction Temperatures	150°C maximum
Operating Temperature	0°C to 70°C Case

c. Design and Performance Analysis. The preamplifier consists of two Class A stages giving approximately 19-dB gain. Devices being considered for this subsystem require 20 volts dc at $\simeq$ 80 mW. At least one of these devices may be mounted directly on the substrate, reducing the number of separate circuits required.

Following the preamplifier is a driver amplifier consisting of two Class C stages with approximately 15-dB gain. The output of this subsystem is approximately 3 W. Between 1 and 2 GHz nearly all power devices are common base, which would necessitate use of a negative bias voltage if Class B operation were to be proposed. The Class C driver will operate off +24 volts at $\simeq$ 350 mA.

The final subsystem in the module is a combination PA/power control circuit. For the worst-case operating frequency, 1860 to 2000 MHz, this stage could be realized using a commercially available transistor device. This device is well suited for the ARPA radio requirements since it is small (internally matched) and has high collector efficiency (55 percent typical). The typical output of this device is 12 W, leaving 0.8-dB margin for obtaining 10 W at worst-case temperature and

vswr. Experience with a 5-W amplifier (which contains a transistor similar to the devices planned to be used) shows that as much as 1-dB power sag may be experienced.

The power control circuit is shown in figure 8.3-10. Two attenuators are used, one preceding and one following the PA. Each attenuator may be stepped twice. The input attenuator would be stepped first, lowering drive to the Class C PA. With these first two attenuation steps, the PA current would decrease with output power. A maximum of 10 to 12 dB may be stepped in before the Class C stage turns off. The output attenuator causes no current drop, but greatly increases the dynamic range of power control. Stepping it after use of the input attenuator allows the output attenuator to be designed at a 1-W level, allowing less

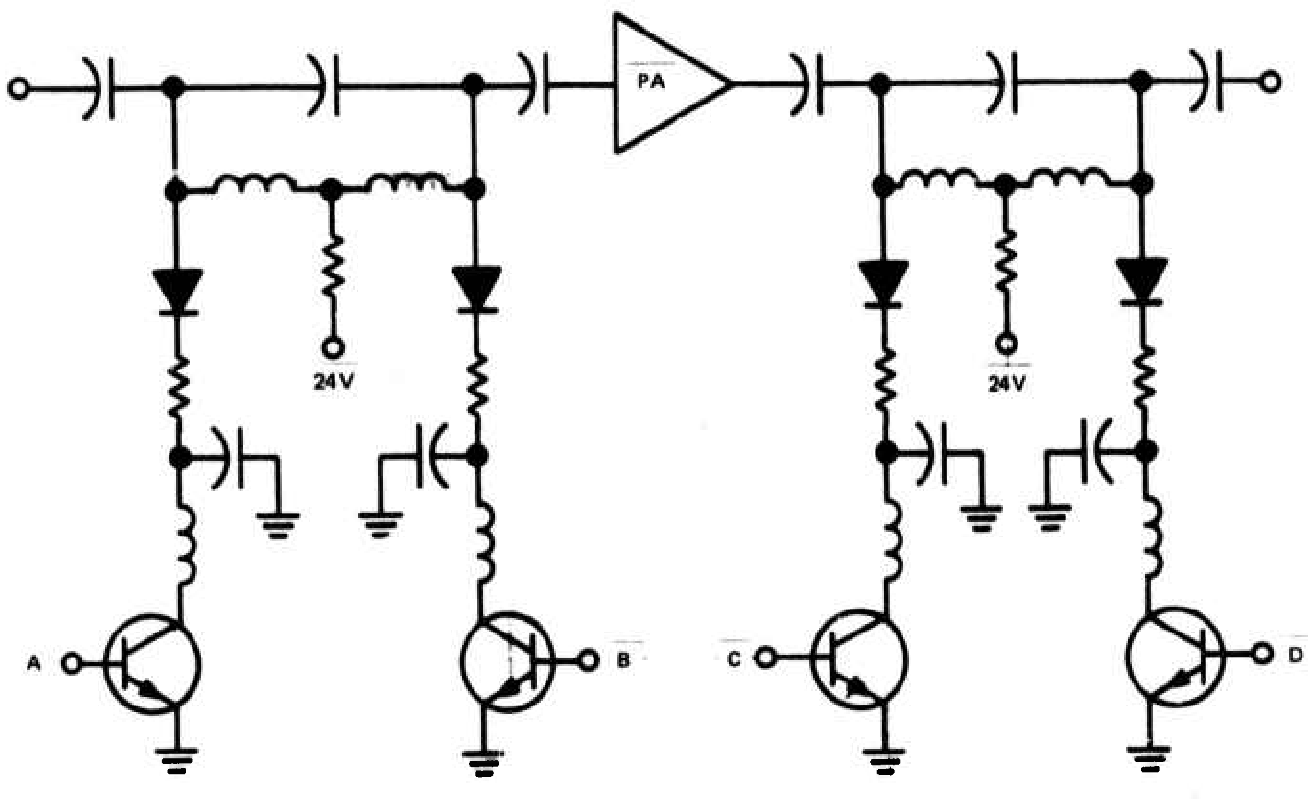


Figure 8.3-10. Power Control.

attenuator current and less expensive devices. Devices being considered are 1-W microwave pin diodes in a stripline package with heatsink. Since the pin diodes are used in shunt, their only effect while biased off is their shunt capacitance. The pin diode devices are rated at 0.12 pF, giving negligible effect at 2 GHz. Each pin diode required +5 volts at 20 mA when attenuating.

In addition to the above circuitry, a bias control switch will be furnished that turns off the bias to the Class A stage during receive mode (see figure 8.3-11). Only minimal base current is required at 5 volts to drive the switch.

d. Packaging Data. The power amplifier and power control circuitry will be contained in a single moisture-sealed package. The majority (if not all) of the circuitry will be of hybrid microstrip design. Hermetically packaged semiconductors will be used, but there will be no attempt to make the entire module hermetic. Figures 8.3-12 and 8.3-13 give maximum dimensions and a tentative layout scheme for the module. Layout details (such as connector locations) are to be specified. If possible, switching circuitry will be incorporated with the alumina circuits using no printed wiring board type assemblies. Paragraph 8.3.4.3 shows the PA incorporated into an rf head assembly that can be used in any network terminal/repeater/station configuration.

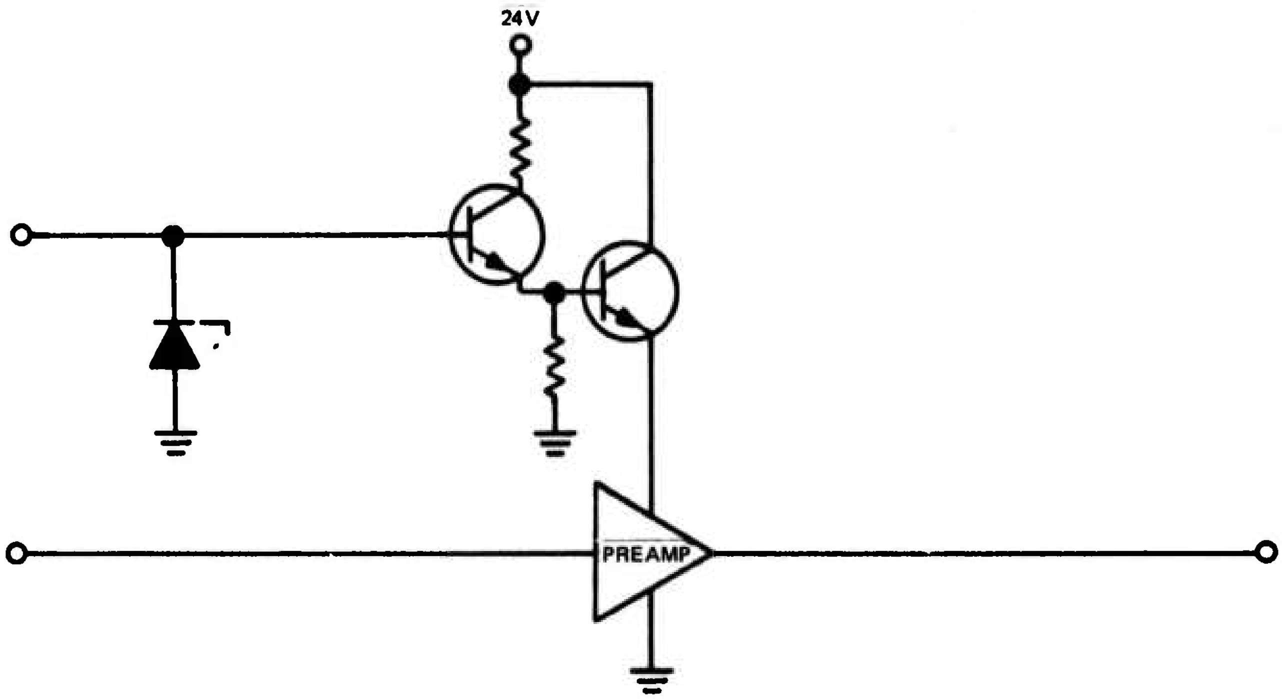


Figure 8.3-11. Power Switch.

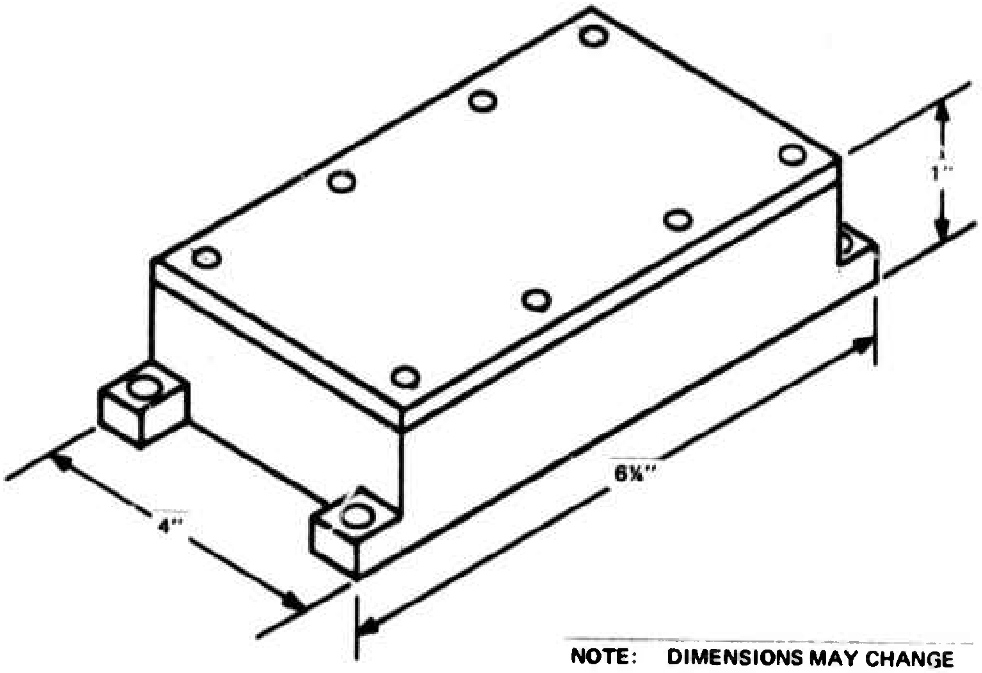


Figure 8.3-12. PA Mechanical Sketch.

e. Control and Monitor Provisions.

1. Control. The power level control requires 0- to 5-volt pulses as defined in the table of figure 8.3-ь. The bias switch also requires 0- to 5-volt pulses, with 0 voltage giving bias on.

2. Monitor. No monitor requirements have been defined for the PA. Current monitors may be easily incorporated. However, a power monitor (such as a coupler in output) will lower output power and increases module size.

f. Power Estimate. 33 W cw. See paragraph b. for duty cycle requirement.

g. Additional Features. 'he electrical configuration of the PA and power control is identified in all termi /repeater/station configurations. For repeater and station applications, additional heatsinking may be required for higher duty cycle usage.

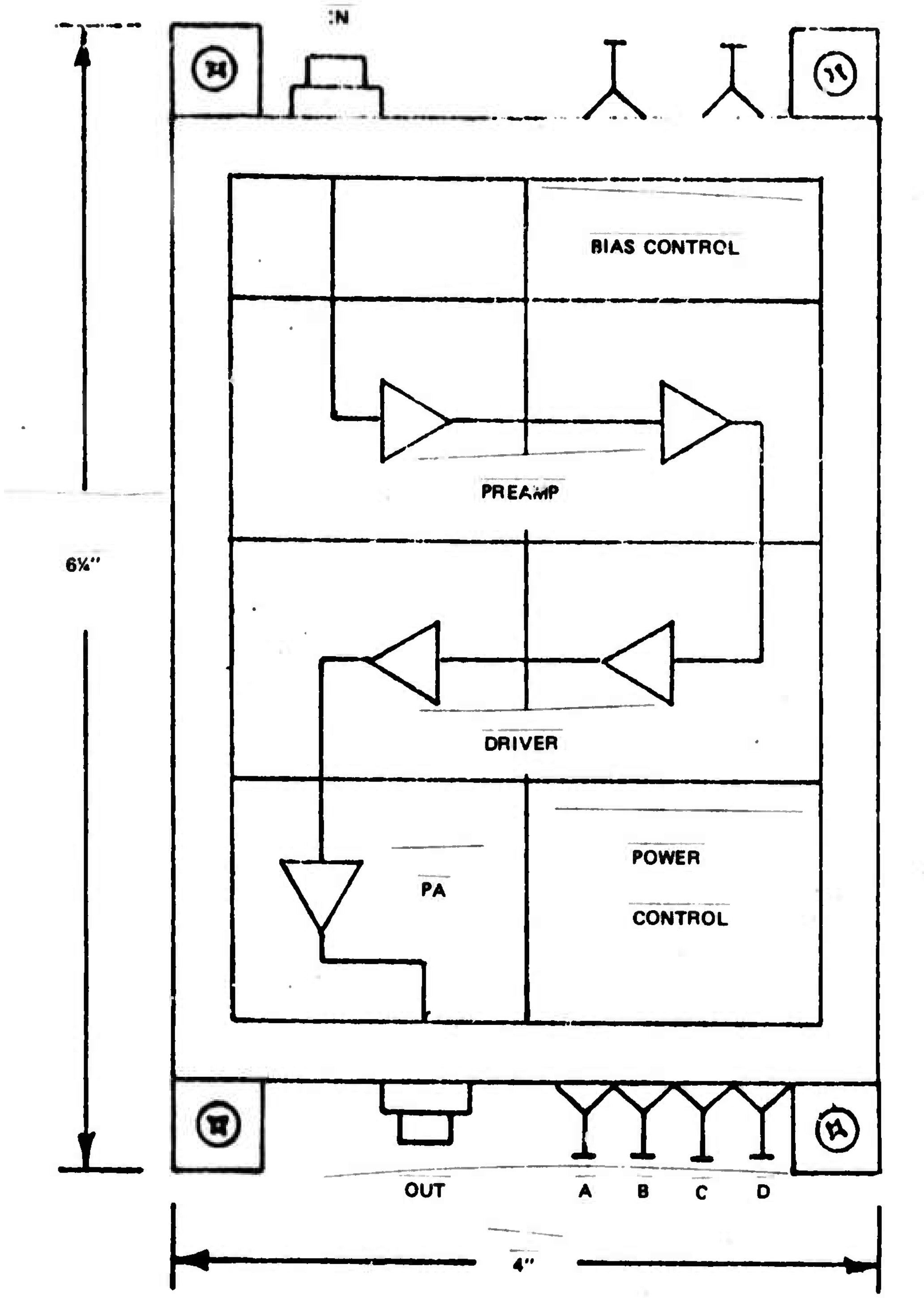


Figure 8.3-13. PA Layout.

8.3.4.4 T/R Switch

a. Functional Description. The T/R switch operates in conjunction with the PA and receiver. When in transmit mode, the T/R switch connects the PA to the antenna and disconnects the receiver functions. In receive mode, the T/R switch connects the receiver to the antenna and disconnects the PA.

The T/R switch consists of a circulator and a PIN diode switch in the receive port of the circulator.

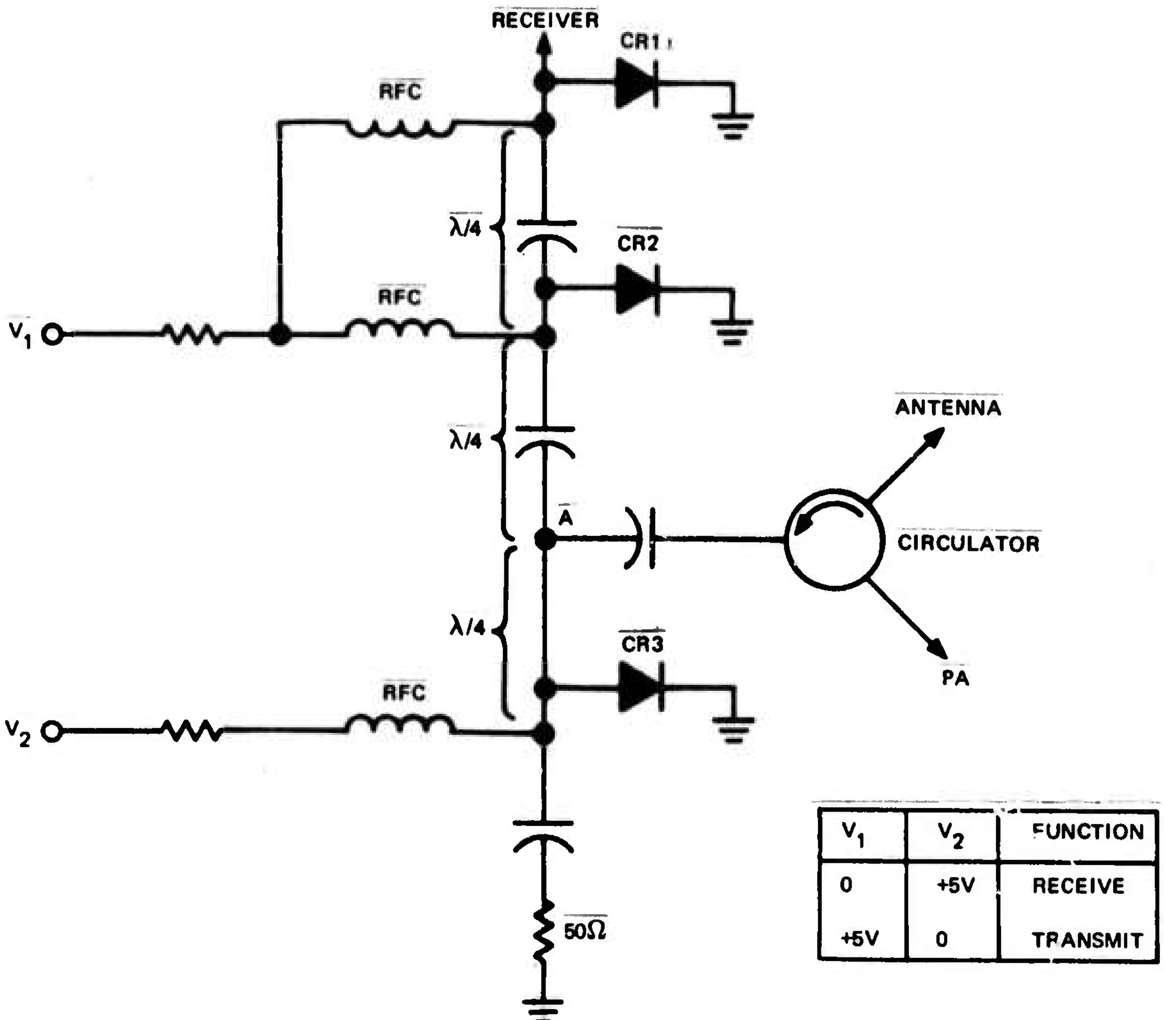
b. Functional Interface

Frequency	1710 to 1850 MHz
Bandwidth	140 MHz
Insertion loss:	
Antenna to Receiver	≤ 1 dB
PA to antenna	≤ 0.5 dB
Isolation	40 dB minimum
Reflected Power Termination	50 Ω , 10 W
VSWR All Ports	$\leq 1.15:1$

c. Design and Performance Analysis. The circulator is a commercially available ferrite disc device. This type circulator mounts in the floor of the chassis with solder tabs connecting directly to alumina circuitry. The circulator gives 20-dB T/R isolation and a good vswr at all ports.

The diode switch consists of pin diodes and bias circuitry. (See figure 8.3-14.) In transmit mode, the control voltage V1 shorts CR1 and CR2 (to $\sim$ 0.8 Ω) and presents an rf open circuit at point A. Meanwhile, V2 remains at 0 volt, turning off CR3 and terminating the circulator in 50 Ω . Note that the receiver will see an rf short. The pin switch gives > 40 dB of isolation. In receive mode, V1 and V2 are reversed, CR 3 is shorted, and the rf path is to the receiver. The insertion loss through the pin switch will be due only to line loss and mismatch due to the OFF diode's shunt capacitance. The devices being considered have a typical shunt capacitance of 0.12 pF, which gives negligible mismatch at 2 GHz. These devices are microwave pin diode modules consisting of a 50 Ω transmission line shunted by a pin diode.

d. Packaging Data. The T/R switch will be packaged in microelectronic form. Size will be approximately 0.75 x 0.20 x 2.5 inches. Refer to paragraph 8.6 for integration into mechanical rf assembly.



V_1	V_2	FUNCTION
0	+5V	RECEIVE
+5V	0	TRANSMIT

Figure 8.3-14. T/R Switch.

e. Control and Monitors. Two control lines are required, one for transmit and one for receive. Signals required are 0 volt off and 5 volts on. Transmit requires 40 mA. at +5 volts and receive control requires 20 mA at +5 volts. Microprocessor interface circuits are required in the rf head mechanical assembly.

f. Power Estimate. 100 mW receive; 200 mW transmit.

g. Additional Features. All T/R switch functions are identical and interchangeable for all network configurations.

8.3.4.5 T/R Filter

a. Functional Description. The T/R filter purpose is twofold. One is to eliminate out-of-band spurious signals when transmitting. The second is signal rejection to the receiver from unwanted signals seen by the antenna.

To meet these requirements, a 5-pole Chebyshev filter is used.

b. Functional Interface.

Frequency Loss Band	1710 to 1850 MHz
Insertion Loss	<0.5 dB
Phase Linearity	±15 degrees over any 20-MHz bandwidth
Impedance	50 Ω
VSWR	<1.2
Out-of-Band Rejection	5-pole Chebyshev filter
Image Rejection	1100 to 1250 MHz; >80 dB
Transmit Power Level	+12 W maximum
Type of Design	An interdigital filter design is proposed but represents a degree of risk. If this filter cannot be realized, a commercially available cavity filter might be used. Its size is approximately 2-3/8 x 1-1/8 x 6 inches. This would affect the packaging approach.
Power dissipation	Depending upon insertion loss, up to 1 W of forward power and possibly 1 W of reflected power under the condition of antenna disconnected.

c. Design and Performance Analysis. The primary requirement of the T/R filter is receiver out-of-band signal rejection, particularly image frequencies. Secondary consideration is transmit up-converter spurious attenuation.

For image rejection, 80 dB is desirable. For a down-conversion scheme to 300 MHz, the image frequencies for low side LO injection is approximately 1100 to 1250 MHz. Figure 8.3-15 shows filter attenuation curves for a 5-pole 0.05-dB ripple Chebyshev filter centered at 1780 MHz. The image frequencies are shown on the curve, and the image rejection is 90 to 100 dB.

Also shown on the curve is the local oscillators. The transmit LO is attenuated by both a 2-pole (in the up-converter) and the 5-pole T/R filter. Total filter LO attenuation is 82 dB minimum, not including up-converter balanced modulation rejection of LO.

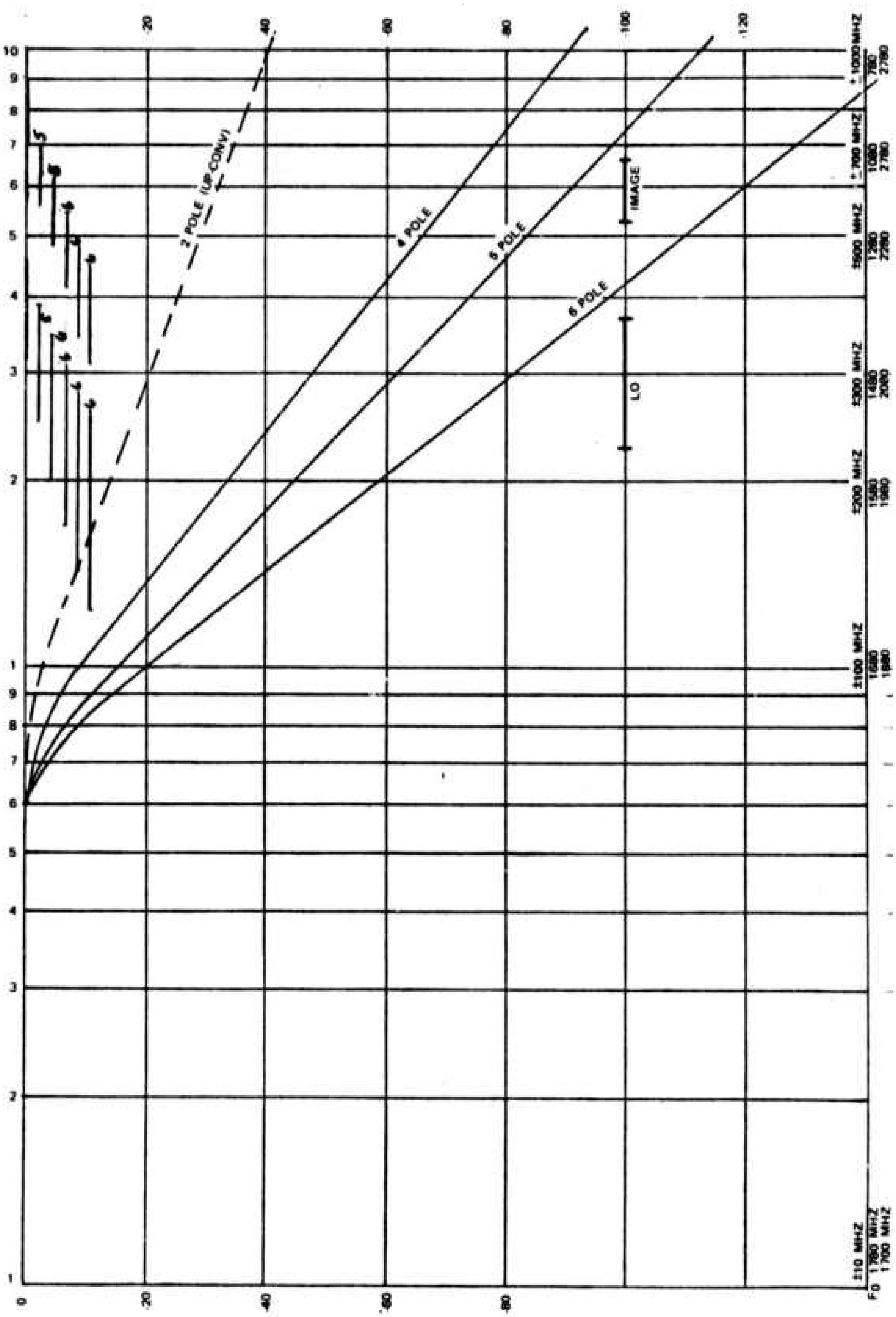


Figure 8.3-15. T/R Filter.

d. Packaging Data. The filter commercially available is 1-1/8 x 2-3/8 x 6 inches. and can meet our specified requirements. An interdigital filter is planned to be developed that is 0.75 x 1 x 2-3/4-inches. Allowances for either configuration is being considered. Refer to paragraph 8.6 for integration of this filter into the mechanical rf assembly.

e. Control and Monitor. None required.

f. Power Estimate. 1-W dissipation maximum if antenna is accidentally disconnected.

g. Additional Features. The same identical and interchangeable filter will be used for all packet radio network configurations.

8.3.4.6 Antenna

Two antennas are described. One is for the repeater application and the other is for the terminal application. The two antennas are described separately, and include a functional description, functional interface, design and performance analysis, and packaging data for each application.

a. Repeater Antenna.

1. Functional Description. The repeater antenna translates rf energy into an omnidirectional, vertically polarized radiation pattern. It also translates radiated received energy in the same fashion.

2. Functional Interface. The interfaces are the channel and the rf head. The channel interface has the following characteristics:

Frequency	9-percent bandwidth in 1- to 2-GHz range
Polarization	Vertical

The rf head interface has the following characteristics:

Frequency	9-percent bandwidth in 1- to 2-GHz range
Maximum Input Power	50 W
Input VSWR	Maximum 2:1 design goal 1.5:1
Connector	Type TNC female

3. Design and Performance Analysis. The antenna consists of two radiating elements each of which is fed at two points, as shown in figure 8.3-16. The elements are sleeve dipoles stacked colinearly. Each element is about 1-1/2 wavelengths long. By feeding at two optimally positioned points, the current along the element can be maintained in-phase providing about the same gain as three colinear dipoles. The main advantage is the reduction of the number of feedpoints. This is important if the diameter of the antenna is to be kept to a small value.

The feed is arranged so that a 50 Ω system is maintained throughout. Type RG-141 is used as the main feed. Two series 25 Ω lines are used as the first branch, and at the outer ends two 50 Ω cables in parallel provide a match. The whole radiating assembly is placed in a fiberglass tube to provide an integral unit that should require no maintenance.

Two design problems exist. They are impedance and patterns.

The impedance of the elements at the design frequency will be high, and a matching network must be provided. In view of the rather small percentage bandwidth, this should not be a formidable problem.

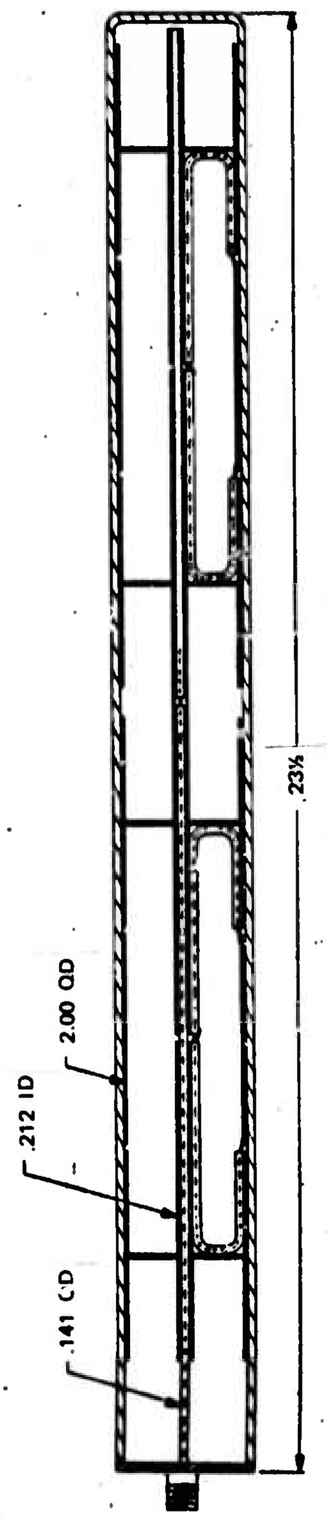


Figure 8.3-16. Repeater Antenna.

The second problem is determining the proper feedpoints. If these locations are not correct, an out-of-phase current will exist on the center part of the element, resulting in severe sidelobes on the patterns. In a colinear element with feedlines extending out the ends of the elements, there is capacity present that makes it difficult to predict the optimum feed length. This is most easily accomplished experimentally. Radiation patterns will be recorded and the feedpoints adjusted so that large sidelobes are present over only a very small band of frequencies and not in the operational band.

Figure 8.3-17 shows a typical pattern for an antenna similar to the one proposed. The gain of the antenna will be 9 dB above isotropic.

4. Packaging Data. The physical size is shown in figure 8.3-16, and it will weigh approximately 5 pounds for the target 1710- to 1850-MHz range.

5. Control and Monitor. None.

6. Power Estimate. None.

7. Additional Features. Repeater and station applications.

b. Terminal Antenna.

1. Functional Description. The terminal antenna has the identical functional description and interface to channel and rf head.

2. Functional Interface. Same as repeater with the exception of the maximum input power which is 25 W.

3. Design and Performance Analysis. The antenna consists of a vertical dipole for use without a ground plane. Removable tripod legs are provided so the antenna may be set on a desktop, or if desirable, longer legs could be provided so the antenna can be placed on the floor. A right angle TNC connector is used so that the cable connection will not try to overturn the antenna.

Because of the small size of this unit, it is made as an integral unit except for the legs. The elements are housed in a rugged fiberglass housing. No external adjustments are provided. For other frequency bands, the length of the antenna will vary inversely as the frequency. It has 0-dB above isotropic gain. This is the major difference in performance between the repeater and terminal antennas.

4. Packaging Data. Figure 8.3-18 shows a cross-section view of the terminal antenna. Figure 8.3-19 shows the physical dimensions for the target frequency band 1710 to 1850 MHz. The weight of this antenna is approximately 5 pounds.

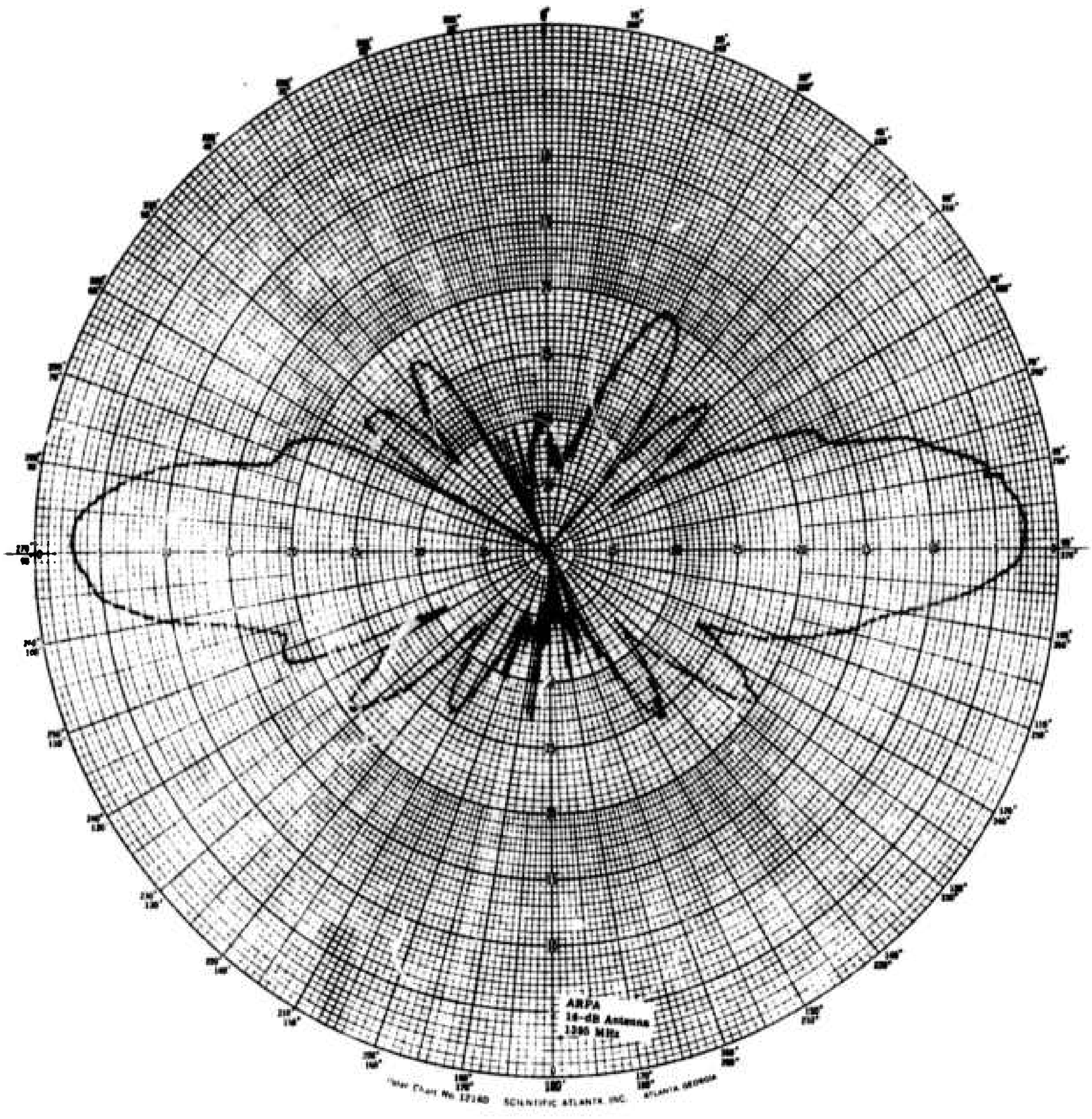


Figure 8.3-17. Typical Antenna Elevation Pattern.

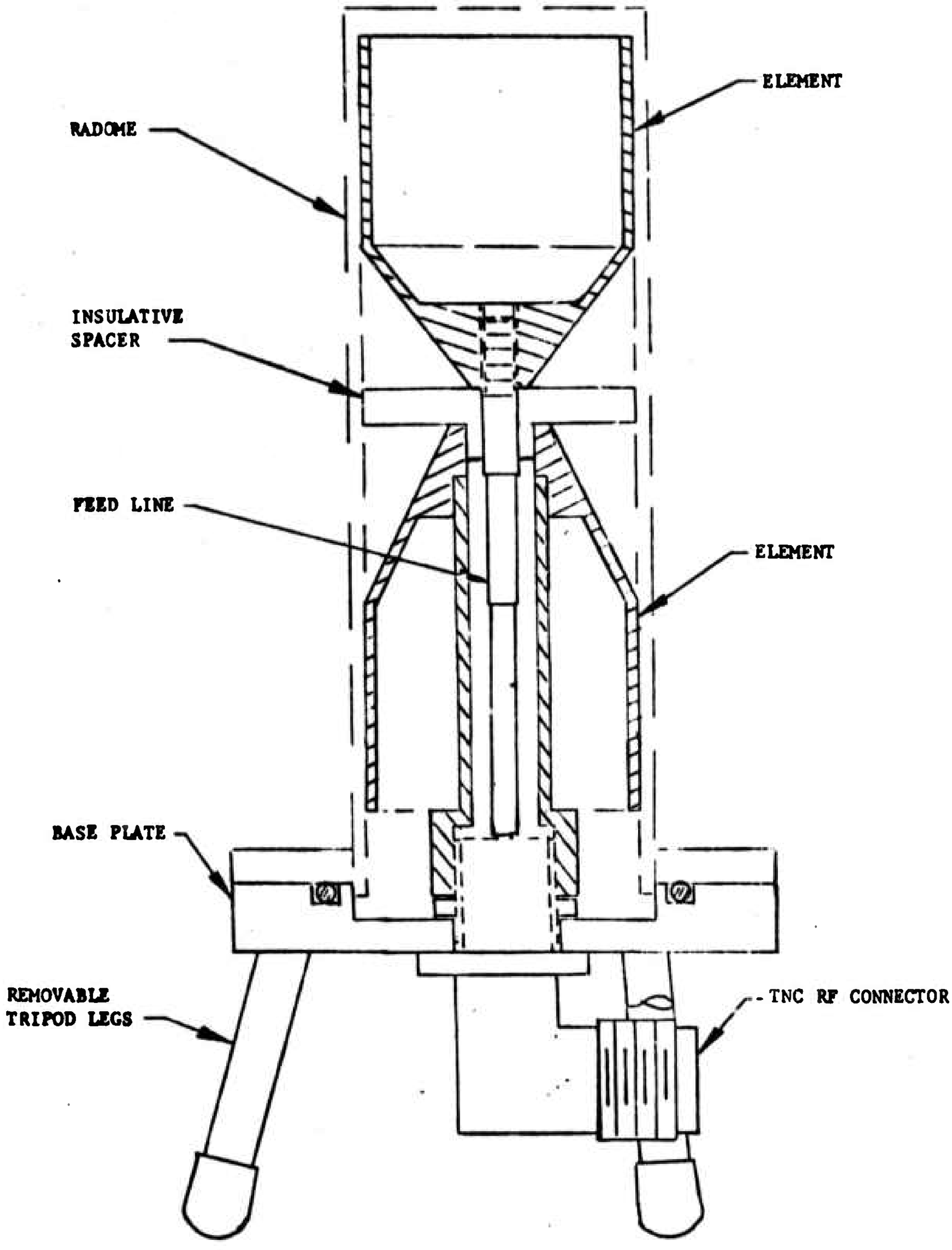


Figure 8.3-18. Terminal Antenna Detail.

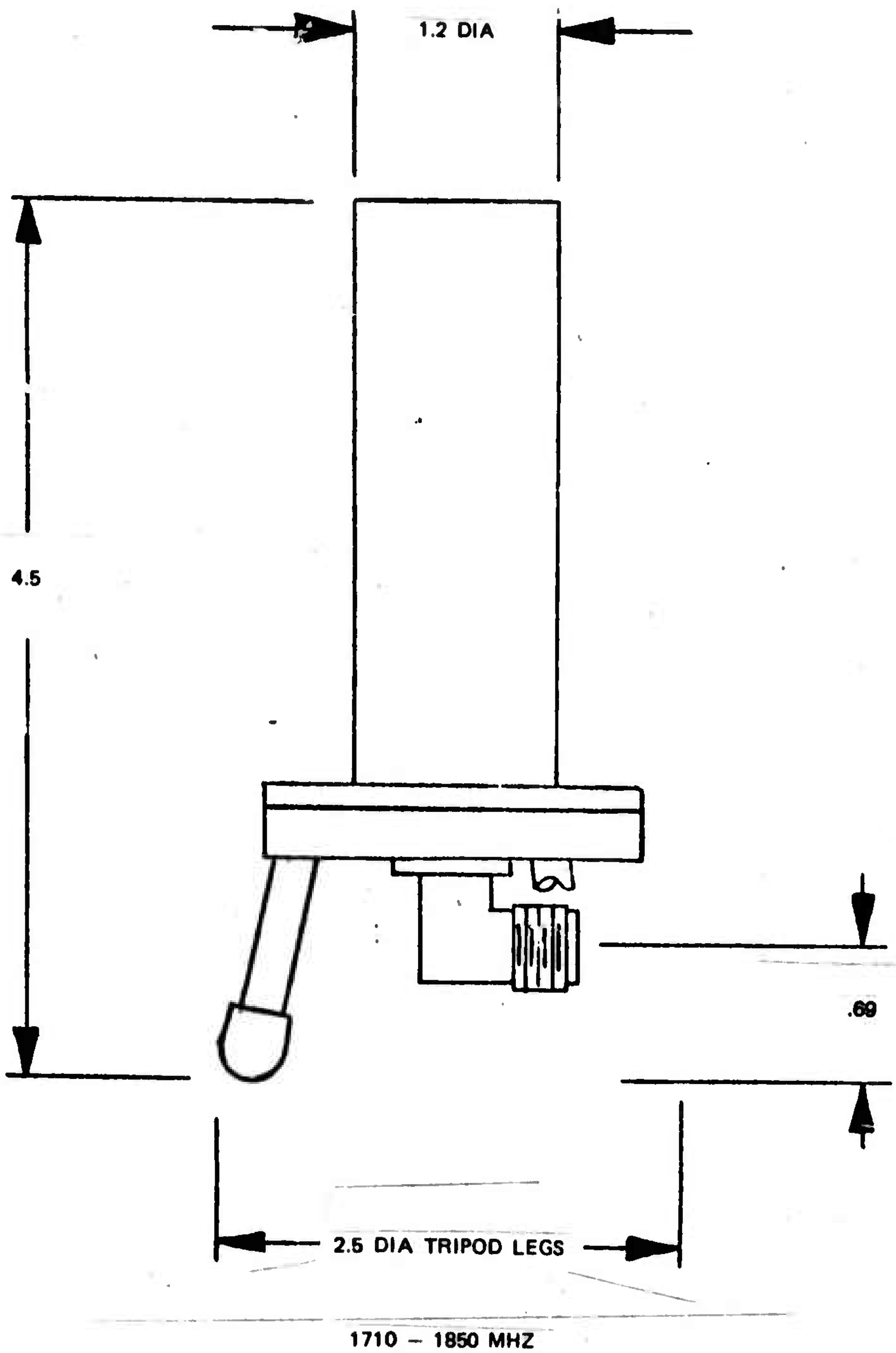


Figure 8.3-19. Terminal Antenna.

8.3.4.7 Frequency Generation

The two requirements of frequency generation are LO (local oscillator) and chip/bit clock frequencies. Because of SAWD requirements, these are generated separately (two frequency standards) although ideal SAWDs permit use of one standard.

a. LO Generation Functional Description. One LO is generated and power split for simultaneous transmit LO and receiver LO use and is illustrated in the right half portion of figure 8.3-20. A digital frequency synthesizer is featured with frequency step size of 6.3 MHz with 10 steps available. Doubling the synthesizer output produces ten 12.6-MHz steps from 1423.800 to 1537.200 MHz. With an if. of 299.250 MHz, this produces an actual rf center frequency of 1723.05 to 1836.45 in 12.600-MHz steps. By moving the standard frequency ±11 ppm, the output frequency may also be moved ±11 ppm, or about ±20 kHz. This allows SAWDs to be ±20 kHz in error.

   The actual frequency is controlled by four control lines from the microprocessor. These control lines program the loop feedback counter divide ratio of ÷113 through ÷122.

   The LO frequency standard must hold its stability (±1 ppm) with temperature with a settability range of ±11 ppm. The frequency is 3.150 MHz, which is in the optimum frequency range of Temperature Compensated Crystal Oscillators (TCXOs) and this component may be easily purchased.

b. Chip/Bit Clock Generation Functional Description. The stable clock generation is a frequency standard followed by various dividers to obtain the required frequencies. All frequency dividers can be implemented easily up to 50 MHz with commercially available integrated circuit dividers.

   The frequency standard is a TCXO operating at 50.4 MHz.

   This TCXO also requires ±1-ppm absolute frequency stability, but does not require a settability range that the other TCXO requires. Therefore, this oscillator would be easier for the component manufacturer to implement but 50.4 MHz does require overtone crystal operation, which complicates the design.

c. Functional Interface.

   1. LO Outputs.

      Two outputs, one transmit and one receive

      P_o = +7(±3) dBm at 50 Ω

      Frequency = 1423.80 through 1537.20 MHz

      Frequency steps = 12.6 MHz

      Frequency switching speed ≤ 1 ms to be within 10 degrees of final phase

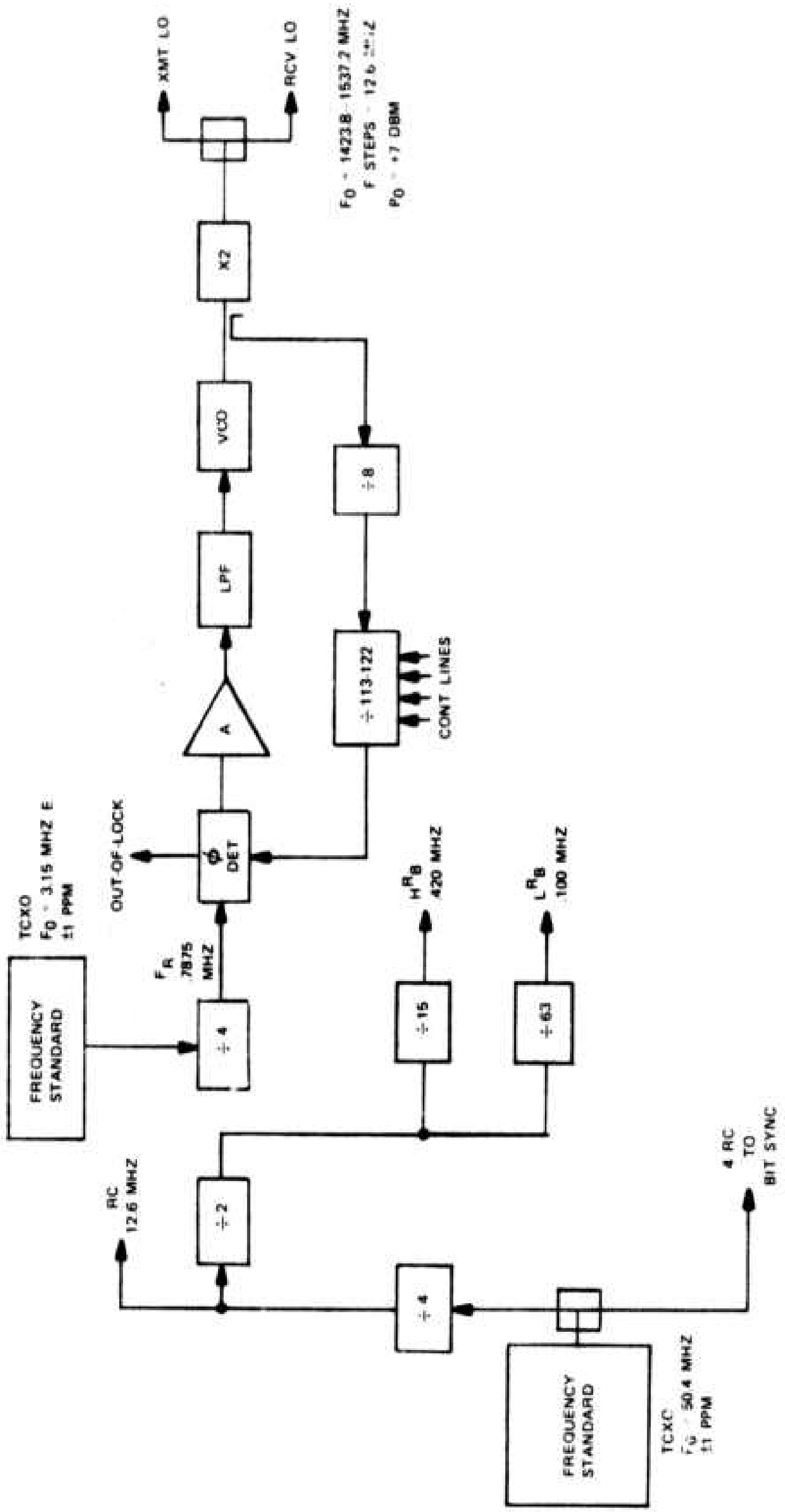


Figure 8.3-20. Frequency Generation.

TCXO stability = ±1 ppm

TCXO settability = ± 11 ppm

2. Control Lines

Four logic lines from microprocessor, whose states corresponds to required output frequency

3. Chip/Bit Clocks.

TCXO Stability = ±1 ppm

$4 R_c$ = 50.4 MHz for bit sync circuitry, ECL interface

R_c = 12.6 MHz, TTL interface

$L^R B$ = 100 kBps clock, COS-MOS levels

$H^R B$ = 420 kBps clock, COS-MOS levels

4. Status Output.

Out-of-lock indicator at COS-MOS level

d. Design and Performance Analysis.

1. Phase Noise and Spurious Output. The main area of concern in any synthesizer is phase noise and spurious output.

A commercially available voltage controlled oscillator (VCO) packaged in a TO-8 can that operates fundamentally at 700 to 800 MHz is used. Its single sideband (ssb) phase noise specification is -65 dB in a 1000-Hz bandwidth. Doubling in the X2 and normalizing to a 1-Hz bandwidth results in -90 dB/Hz. Since 100-kBps data is of interest, phase noise modulation rates of 50 kHz and above predominate. Integrating the VCO noise from 50 kHz to infinity and taking into account double sideband (dsb) and two oscillators (up-convert and down-convert), the resultant signal to total phase noise is 40 dB. This assumes no effects of loop bandwidth. This is valid since loop bandwidth will be in the order of 10 kHz. This is more than adequate for bit error rate (BER) performance.

Spurious signals are frequency synthesizer reference frequency components (787.5 kHz) and power supply ripple and noise components modulating the VCO. The latter is a design problem concerning shielding and supply line filtering. Reference frequency components can be eliminated by loop filtering, but at the expense of requiring lower loop bandwidth and lower switching speeds. With 10-kHz loop bandwidth, 110 dB of loop filtering on 787.5-kHz reference frequency components can easily be obtained. Resultant spurious output is calculated, for small phase deviations, by:

$$E_1/E_c = (X2)\frac{\Delta F}{2fm} = (X2)\frac{EvKv}{2fm} = X2\,\frac{E\phi \propto Kv}{2fm}$$

where

E_1/E_c = sideband to carrier ratio

X2 = Doubler effect

ΔF = Frequency deviation of VCO caused by fm

fm = Modulating frequency = 787.5 kHz

Ev = FM voltage at VCO

Kv = VCO sensitivity in Hz/volt ≃ 25 MHz/volt

E_ϕ = FM voltage at phase detection

α = Filter attenuation at fm ≈ 3 x 10^{-6} (110 dB)

Spurious output is $E_1/E_c \approx$ -66 dB.

which easily satisfies receiver requirements of 50-dB spurious rejection.

2. Loop Program Counter. The ÷ 113-122 divide will be implemented as shown in figure 8.3-21.

The divide operates normally by ÷ 8 x 14 = 112. That is, 14 cycles of ÷ 8-9 occurs for each output cycle. Each cycle of the output strobes the frequency control line into the ADD counter. The ADD counter causes ÷ 9 counts N times, where N is the value of the control lines. Thus, as the equation in figure 8.3-21 suggests, ÷ 9 occurs N times, and the remaining ÷ 8-9 cycles out of 14 divides by 8.

Since the power dissipation of high-speed dividers is quite high, additional circuitry (sample and hold phase detectors, in parallel to dividers) may be used. Once phase lock occurs, the dividers may be dropped (disconnected

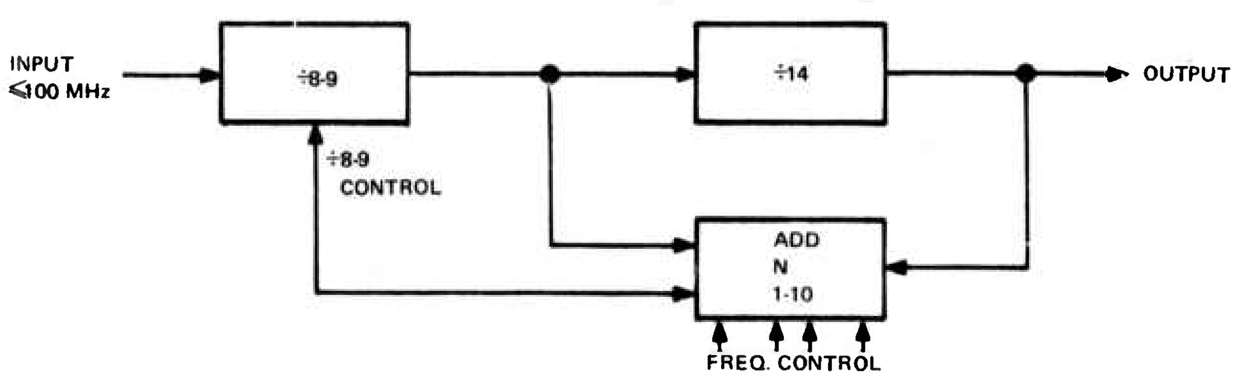


Figure 8.3-21. Program Divider (÷ 113-122).

from power) and the relatively low power sample and hold (S H) circuits may be used to maintain lock. At this time, this technique is not planned to be used.

3. Frequency Standard Stability Analysis. The stability of the TCXO considered is ±1 ppm. The effect of this stability upon expected packet length is considered in this analysis.

Each transmit function has two independent TCXOs, and each receive function (another network radio) has two independent TCXOs. Hence, worst-case overall frequency stability is ±4 ppm. Each oscillator variance is 0.3 ppm (assuming $3\sigma = 1$ ppm). Then, the total variance is

$$\sigma_T = \sqrt{\sigma_1^2 + \sigma_2^2 + \sigma_3^2 + \sigma_4^2} = 2\sigma = 0.6 \text{ ppm}.$$

Over the expected packet length of 2048 bits, at 100 kBps, the time is 20.48 ms. The variance of bit timing at the end of packet would be 0.6 ppm times 20.48 ms = 12 ns. The worst-case clock error would be 82 ns. Adding 20-ns worst case, and 10-ns variance tolerance due to receive bit timing being initially adjusted (at end of preamble) in 20-ns increments, the total error would be 15.6-ns variance and 102-ns worst-case error. Since the data detectors using a timing sample window of ±2Tc (±158 ns), the assumed frequency standard stabilities are quite satisfactory to meet system performance objectives.

Additionally, short term stability of the oscillator must also be considered. 10^{-8} stabilities for 1 second and less are easily obtained. For 20 ms this results in 0.8-ns worst case. Therefore, short-term stability is not a serious consideration. Only the long-term drift between standards is of importance.

e. Packaging Data. Packaging will be printed circuit card construction with certain functions such as VCO and X2 doubler in shielded compartments. Total circuit area is estimated to be 49 in.^{2}, including connectors, shielding, mechanical interfaces, etc.

f. Power Estimate.

	(Area (in.)	Power (mW)
Frequency Standard	4	300
Power Split	1	-
÷4 (SP601A)	1	90
÷2 (SP602)	1	60
÷3 (LP-TTL)	1	40

	Area (in.)	Power (mW)
÷5	2	80
÷21	3	120
÷ 8 (SP609B 601A)	3	290
÷113-122	10	1500
DET	3	60
÷4	1	40
Frequency Standard	4	300
AMP	2	100
LPF	3	-
VCO	2	750
X2	4	500
Regulators (3)	6	100
TOTAL	49 $in.^2$	4.33^W

g. Control and Monitor. For the frequency generator, there is one control function and one monitor function available to the radio interface.

The control function is the four lines that program frequency.

The monitor function is the out-of-lock line available from the synthesizer phase-detector. The 0-0-L function monitors the synthesizer loop for lock status.

h. Additional Features. The requirement that differs for the frequency generation for terminal, repeater, and station environments is the requirement that high-rate bit clock does not need to be generated in the terminal application. However, this requirement is negligible on circuit complexity and power dissipation.

Hence, all applications (terminals, repeaters, and stations) will use identical and interchangeable frequency generation functional modules.

8.3.4.8 Down-Converter

a. Functional Description. The down-converter is functionally shown in figure 8.3-22. Its function is to convert the rf (1723.05 to 1836.45 MHz), received from the T/R switch to the if. (299.25 MHz). This is accomplished by first preamplifying the rf signal and then mixing the same in a doubly balanced mixer with the receiver LO frequency (1423.8 to 1537.2 MHz). The output of the mixer is filtered through a 20 MHz wide, 5-pole Chebyshev, bandpass filter centered at 299.25 MHz. The filter rejects the spurious frequencies including the upper sideband frequency. The filtered if. is preamplified before it goes out of the down-converter to the agc amplifier.

b. Functional Interfaces.

RF Input	1723.05 to 1836.45 MHz msk
Power	-100 to 0 dBm
NF≤	8.2 dB
LO Input	1423.8 to 1537.2 MHz
Power	+7(±3) dBm
IF Output	299.25 MHz msk
Bandwidth	20 MHz
P_0	-88 to 0 dBm

c. Design and Performance Analysis. In this subsection it is shown that the power levels in spurious frequencies from the mixer are sufficiently suppressed due to the inherent IMP rejection capability of the mixer combined with the attenuation characteristic of the 5-pole Chebyshev filter to out-of-band frequencies. The noise figure (NF) for the down-converter elements is also computed.

A chart of difference mixing that plots f_o as a function of the f_L/f_H ratio, and the percentage separation is provided for reference in figure 8.3-23. Of the two frequencies combined in the mixer, f_L is the lower and f_H is the higher frequency. In our case, f_L refers to the LO frequency (1423.8 to 1537.2-MHz range), and f_H refers to the received rf frequency (1723.05 to 1836.45 MHz).

Then, f_L/f_H corresponding to the lowest points of the two frequency ranges = 1423.8/1723.05 (= 0.826) and f_L/f_H corresponding to the highest points of the two frequency ranges = 1537.2/1836.45 (= 0.837).

Now, for whatever rf frequency is to be received, the LO is always to generate its corresponding frequency such that the difference of the two frequencies is the

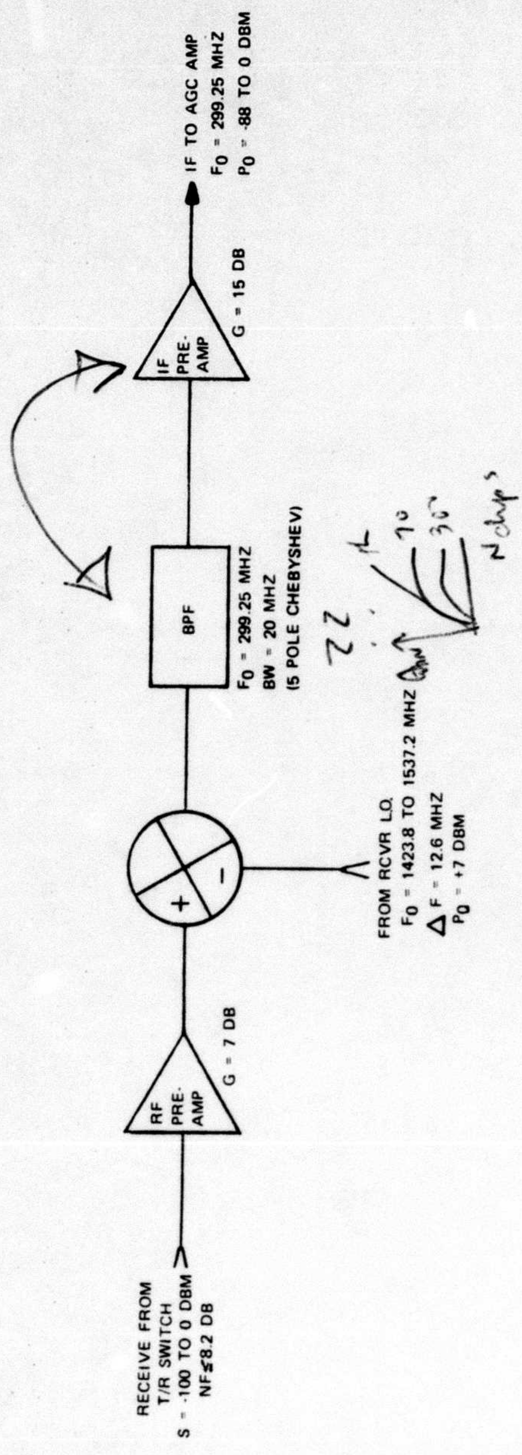


Figure 8.3-22. Down-Converter.

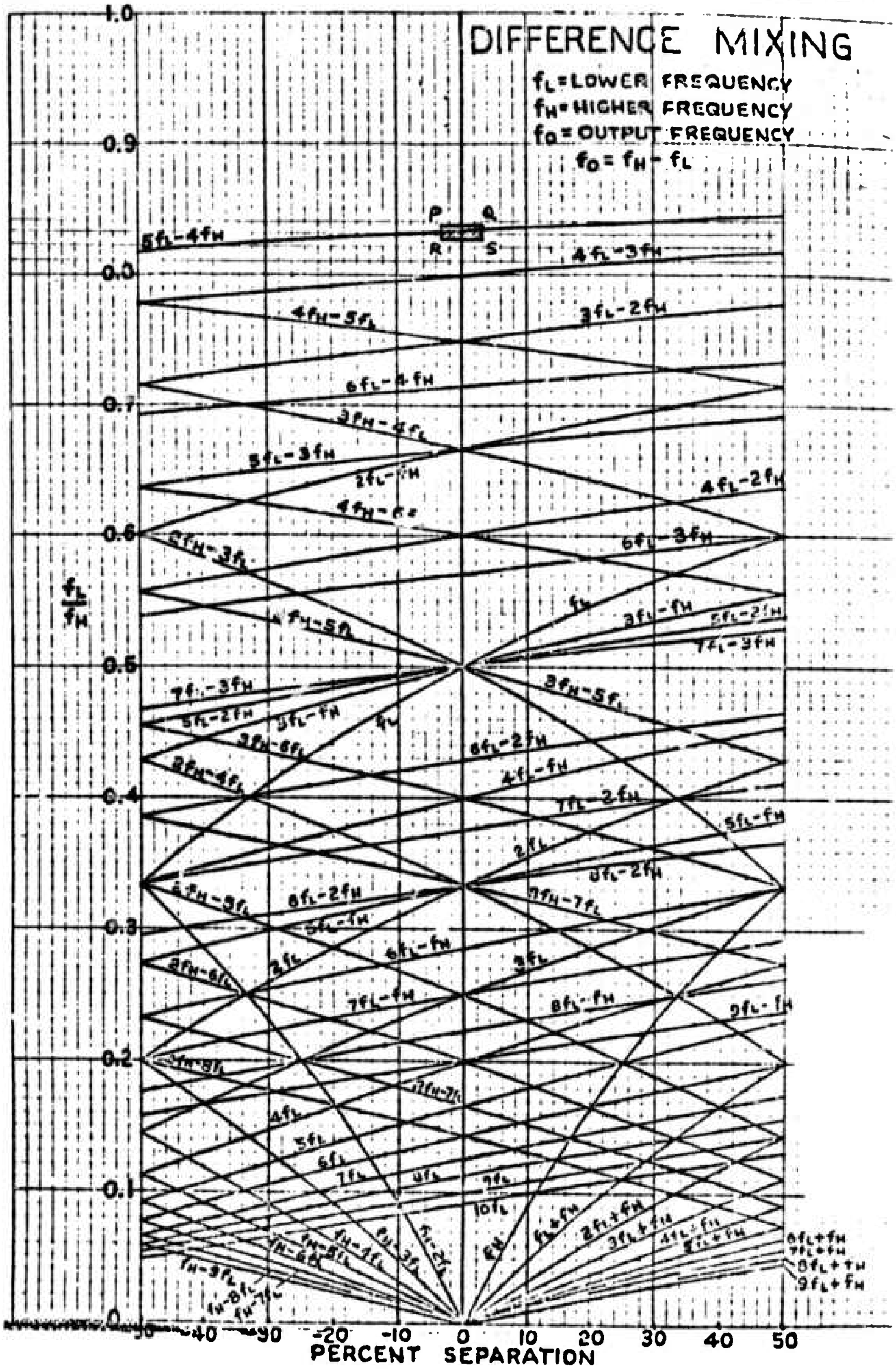


Figure 8.3-23. Receiver IMP Chart.

desired if. frequency (299.25 MHz), which is also the center frequency of the down-converter filter. The lower and upper sideband frequencies of the filter are 289.25 MHz and 309.25 MHz, respectively; 299.25 MHz is +3.34 percent away from the 289.25-MHz sideband frequency and -3.34 percent away from the upper sideband frequency. This separation range is constant for the full range of f_L/f_H ratio from 0.826 to 0.837. Therefore, a rectangle PQRS can be drawn on figure 8.3-23. P corresponds to f_L/f_H of 0.837 at -3.34-percent separation, Q corresponds to f_L/f_H of 0.837 at +3.34-percent separation, R corresponds to f_L/f_H of 0.826 at -3.34-percent separation and S corresponds to f_L/f_H of 0.826 at +3.34-percent separation.

As obvious from the figure, the intermodulated product line $5f_L - 4f_H$ falls within the rectangle PQRS. This line refers to an if. range of 226.8 to 340.2 MHz, corresponding to the full ranges of both f_H and f_L. It is apparent that this if. range will not find always attenuation through the down converted filter; however, the associated order of IMP is such that about 64-dB rejection in the mixer can be expected simply due to the high order of this IMP. (See figure 8.3-24.)

An estimate of power in the spurious frequencies can be obtained from table 8.3-2.

In order to estimate the range of interfering frequencies, recall that the T/R front-end filter 3 dB frequencies are 1710 MHz and 1850 MHz. Therefore, corresponding to the LO range of 1423.8 to 1537.2 MHz, the f_L/f_H ratio within the upper and the lower 3 dB points of the front-end filter varies from 0.76 to 0.898. Hence, the IMP lines labeled as $4f_L - 3f_H$, $4f_H - 5f_L$, and $3f_L - 2f_H$ in figure 8.3-23 are also important to consider since the range of interfering f_H (1695 to 2077 MHz) corresponding to the range of ratios from 0.74 to 0.84 could conceivably result in IMPs that would result in if. Based on figure 8.3-24, table 8.3-3 shows the IMP rejection levels corresponding to the different interfering frequency ranges.

The noise figure (NF) of the down-converter is computed as follows:

Let

F = Noise factor of the down-converter (numeric)

F_1 = Noise factor of the input preamplifier (numeric)

F_2 = Noise factor of the mixer (numeric)

F_3 = Noise factor of the filter (numeric)

F_4 = Noise factor of the output preamplifier (numeric)

	f_L	$2f_L$	$3f_L$	$4f_L$	$5f_L$
$5f_H$				71	56
$4f_H$			62	65	64
$3f_H$		63	60	48	
$2f_H$	33	56	46		
f_H	0	21			

IMP REJECTION IN DB

TYPICALLY FOR f_L AND f_R OF 2 TO 4 GHZ

IF = 100 TO 600 MHZ

f_H AT -10 DBM

f_L AT +7 DBM

Figure 8.3-24. IMP Rejection Levels.

F_5 = Noise factor of the agc (numeric)

G_1 = Gain of input preamplifier (numeric)

G_2 = Gain of mixer (numeric)

G_3 = Gain of filter (numeric)

G_4 = Gain of output preamplifier (numeric)

Table 8.3-2. Receiver IMP Levels.

FREQUENCY (MHz)	*IMP LEVEL AT MIXER OUTPUT (dB)	FILTER ATTENUATION (dB)
$f_L + f_H$ = 3146.85 to 3373.65	0	over 200
$5f_L - 4f_H$ = 226.8 to 340.2	-60	almost none
f_L = 1423.8 to 1537.2	-6 to +87	over 200
f_H = 1723.05 to 1836.45	-20	over 200
*Referred to the desired if. level at the output of the mixer.		

Table 8.3-3. IMP Rejection Levels.

RATIO f_L/f_H	INTERFERING f_H RANGE (MHz)	IMP TYPE	IMP REJECTION (dB)
0.82 - 0.84	1695 - 1875	$5f_L - 4f_H$	64
0.79 - 0.81	1758 - 1946	$4f_L - 3f_H$	48
0.74 - 0.76	1873 - 2077	$4f_H - 5f_L$ &	64
		$3f_L - 2f_H$	46

Then,

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \frac{F_5 - 1}{G_1 G_2 G_3 G_4}$$

$$F_1 = \log^{-1}(5/10) = 3.16$$

$$F_2 = \log^{-1}(7/10) = 5.0$$

$$F_3 = \log^{-1}(3/10) = 2.0$$

$$F_4 = \log^{-1}(2.5/10) = 1.77$$

$$F_5 = \log^{-1}(2.5/10) = 1.77$$

$$G_1 = \log^{-1}(7/10) = 5.0$$

$$G_2 = \frac{1}{\log^{-1}(7/10)} = 0.2$$

$$G_3 = \frac{1}{\log^{-1}(3/10)} = 0.5$$

$$G_4 = \log^{-1}(15/10) = 31.6$$

Calculating $F = 3.16 + \frac{5-1}{5} + \frac{2-1}{5x0.2} + \frac{1.77-1}{5x0.2x0.5} + \frac{3.16-1}{5x0.2x0.5x31.6}$

$$= 3.16 + 0.8 + 1.0 + 1.54 + 0.136$$

$$= 6.636$$

$$NF = 10 \log 6.636 = 8.22 \text{ dB}$$

d. Packaging Data. The size of the down-converter is estimated to be 4 x 1 x 0.75 inches. It is expected that the converter can be built using microelectronic hybrid techniques.

e. Control and Monitor. None.

f. Power Estimate. 20 mA at +15 volts dc

g. Additional Features. Down-converter for all network configurations (terminal/repeater/station) will be identical and interchangeable.

8.3.4.9 AGC Amplifiers

a. Functional Description. Two types of agc amplifiers are used: coherent and noncoherent. Both require essentially the same building blocks. The noncoherent agc is before the SAWD and is intended to amplify the received signals, including interferers, to a composite level of -20 dBm. This may mean that the desired signal is below this level. The amplifier is designed not to saturate. The coherent agc amplifier after the SAWD controls the gain to maintain a constant correlation peak level. Thus, if there is an interferer, the input to the SAWD is lower than desired, but the gain is restored after the SAWD. This two-stage approach reduces the dynamic range requirements of a single amplifier and allows independent control of composite rf levels and correlation peak levels. Both agc's have a store or hold capability so that after the preamble is received, they can be held constant during the reception of message text. The coherent agc circuits also have a blanking feature (optional) for multiple detector use.

b. Functional Interfaces. Figures 8.3-25 and 8.3-26 are the functional diagrams of the noncoherent and coherent agc amplifiers. The interfaces shown on the diagrams are as follow.

1. Noncoherent AGC.

<u>RF Connections</u>

AMP input from down-converter

AMP output to SAWDs

<u>Power and Control</u>

+15 volts dc

-15 volts dc

EOP (End of Preamble) which causes the gain to hold constant.

+5 volts   Hold gain

0 volt   Allow agc action

RCVR Enable

0 disabled

+5 volts enabled

2. Coherent AGC.

<u>RF Connections</u>

Input A from SAWDs

Input B from SAWDs

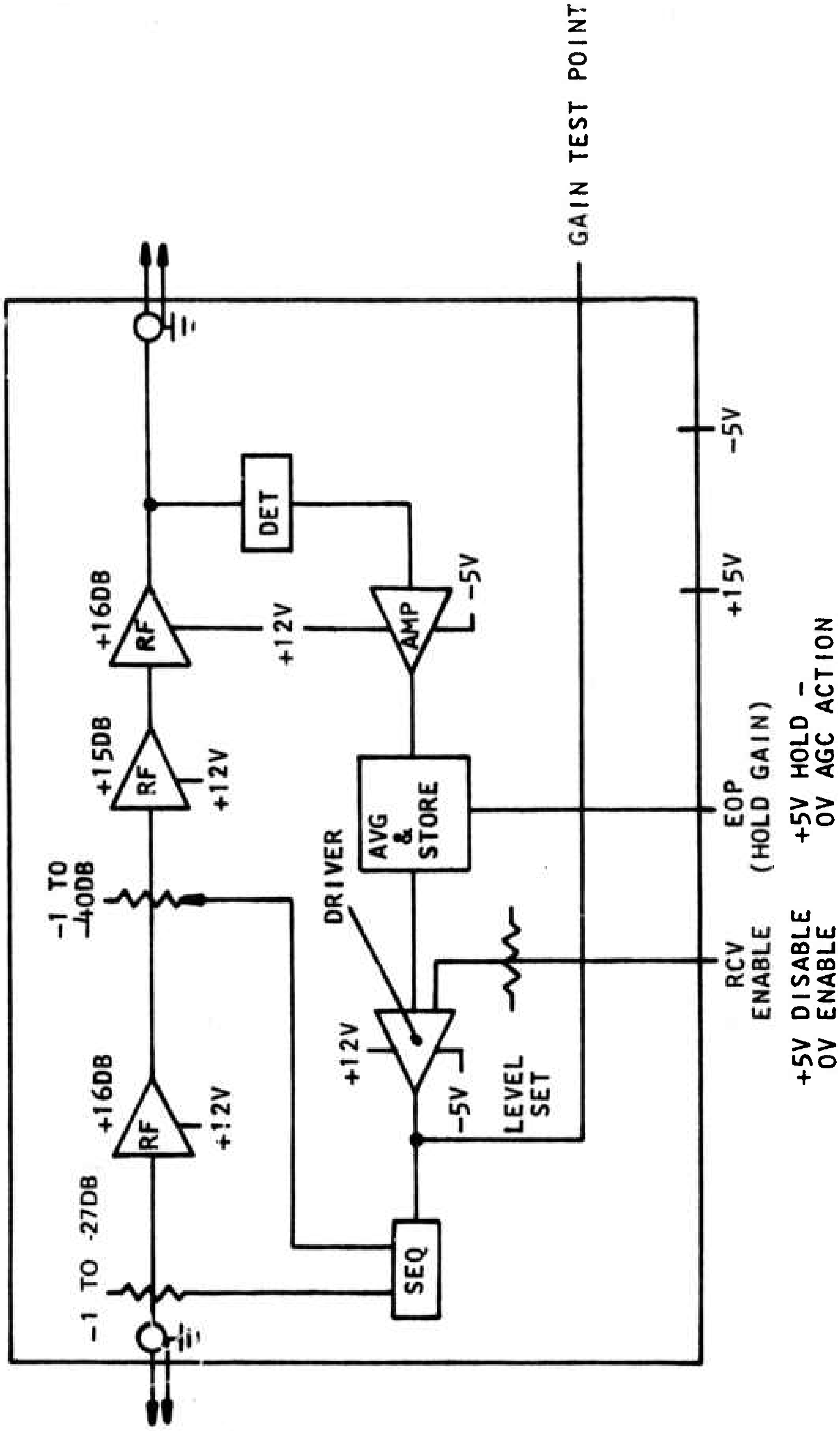


Figure 8.3-25. IF Noncoherent AGC Amplifier.

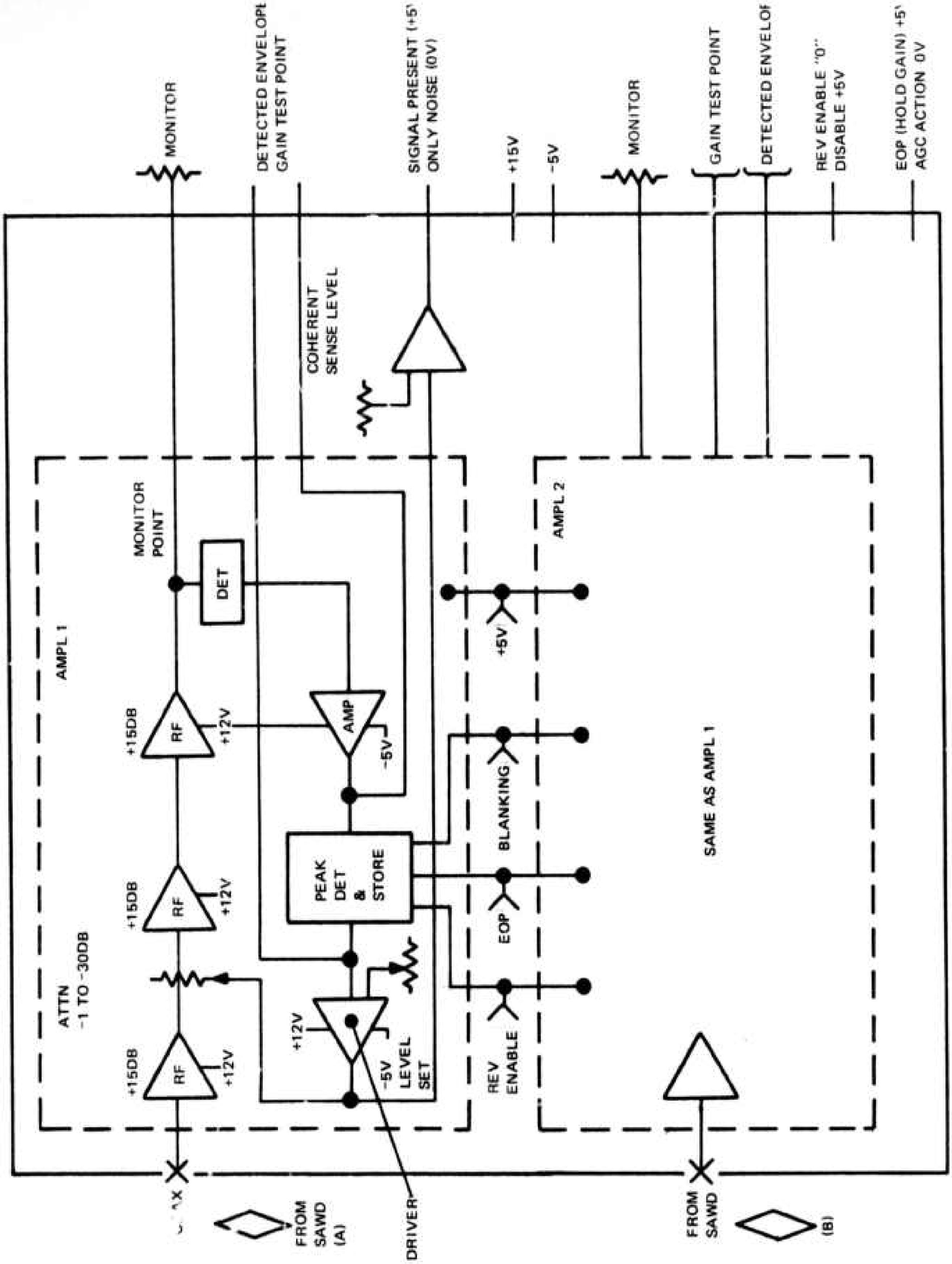


Figure 8.3-26. SAWD Coherent AGC Amplifier.

Power and Control

+15 volts	
-5 volts	
EOP	Same as noncoherent agc
RCVR Enable	Same as noncoherent agc
Blanking	Output
Coherent Carrier Sense	Output

All interfaces with the microprocessor are CMOS levels.

c. Design and Performance. Figure 8.3-27 is a signal-gain-loss analysis for the coherent and noncoherent agc amplifiers. The total maximum gain is fixed to ensure that noise alone will not provide a -10-dBm signal level out of the coherent agc amplifier. A -15-dBm level ±2 dB at this point will be used to indicate that an inband signal is present. Some problems could arise in using the resultant "signal present" output, since it represents either a packet communication or an inband interferer without any differentiation. This signal (coherent carrier sense) is intended to inhibit the XMTR from being keyed.

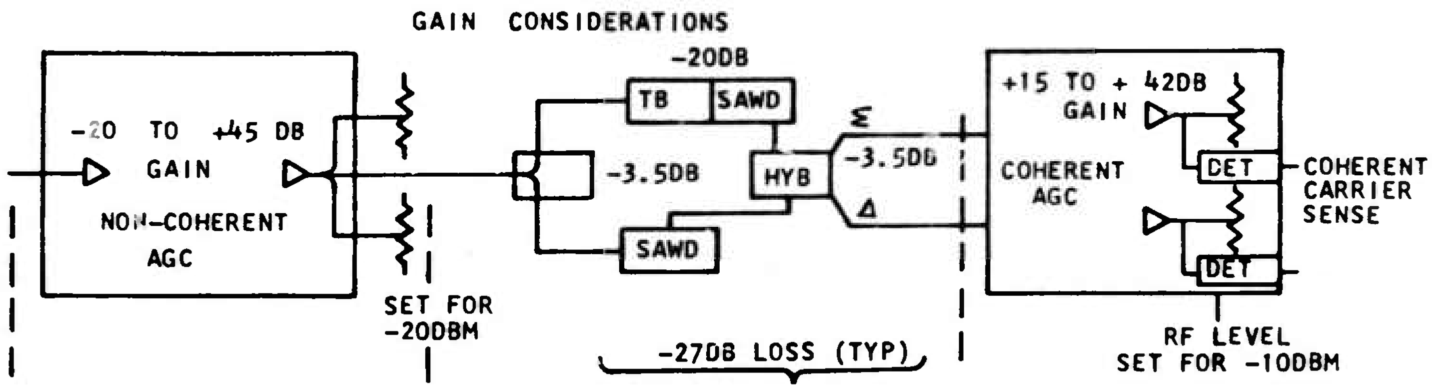
The noncoherent agc amplifier will be set to a composite signal of -20 dBm. The coherent agc amplifier will regulate the peak rf level before detection to -10 dBm.

A review of figures 8.3-25 and 8.3-26 shows the two amplifiers to be very similar. The if. noncoherent agc amplifier has an additional attenuator stage and a drive network to cause the attenuation to react progressive. This will improve the noise figure over the operating range. The average and store circuit will be different from the peak detection and store circuit of the coherent agc amplifier. Both amplifiers will use a low noise rf input amplifier (NF $\leq$ 5 dB) and gain of 15 dB. Table 8.3-4 is a performance summary of a typical commercially available device.

The device is packaged in a TO-5 can with the feature that the chip can be easily extracted from the can and be used on a substrate for microstrip application.

The attenuators are π pin diode networks. Figure 8.3-28 shows the typical configuration. Pin diodes will most likely be used on a circuit board or substrate. Figure 8.3-29 shows the attenuator performance in terms of attenuation and transmission phase angle. The data was taken with a fixed bias on the two shunt pin diodes which provides 20 dB of attenuation.

For the detector circuit, one must look at the data rate and number of bits in the preamble. At the 100 kBps data rate, 10 μs are required per bit (400 kBps, 2.5 μs/bit). The preamble will be 39 bits total length, consisting of 13 bits of Barker code, 13 bits of Barker code inverted, followed by 13 bits of Barker code. Of the last 26 bits, 21 must be correct to detect a valid preamble. In order for the agc levels to stabilize and bit sync to lock up, 13 bits of Barker code preceding the



INPUT (DBM)	NON-COH AGC GAIN (DB)	OUTPUT (DBM)	PROCESSING GAIN (DB)	INPUT (DBM)	COH AGC GAIN (DB)	OUTPUT (DBM)
1) NOISE -80	+45	-35	-27	-62	+42	-20
2) NOISE -80 SIGNAL -90	+45	-35 -45	-27 - 7	-62 -52	 +42	-20 -10
3) NOISE -80 INTERFERROR -50 SIGNAL -60	+30	-40 -20 -30	-27 -27 -7	-67 -47 -37	 +27	-40 -20 -10
4) NOISE 80 INTERFERROR 0 SIGNAL -10	-20	-100 -20 -30	-27 -27 -7	-127 -47 -37	 +27	-100 -20 -10
5) SIGNAL 0	-20	-20	-7	-27	+17	-10
6) NO SIGNAL - NOISE -80 INTERFERROR -70	 +45	 -35 -25	 -27 -27	 -62 -52	 +42	 -20 -10

Figure 8.3-27. Gain Considerations.

26 bits are allowed. The agc must stabilize in advance of the 26-bit preamble identification code. This allows a maximum of about 30 μs at the high data rate and about 130 μs at the low data rate. The coherent agc amplifiers (two required) will be designed to gain stabilize to within ±2 dB of its final value within 20 μs for the high data rate and 85 μs for the low data rate. The noncoherent agc will operate faster. The detector in the coherent agc amplifier must follow the data pulse and integrate the peaks of these pulses to establish the agc level. At the end of a packet, the agc must release in less than 20 μs for the high data rate and 85 μs for the low data rate.

ATTENUATOR NETWORK

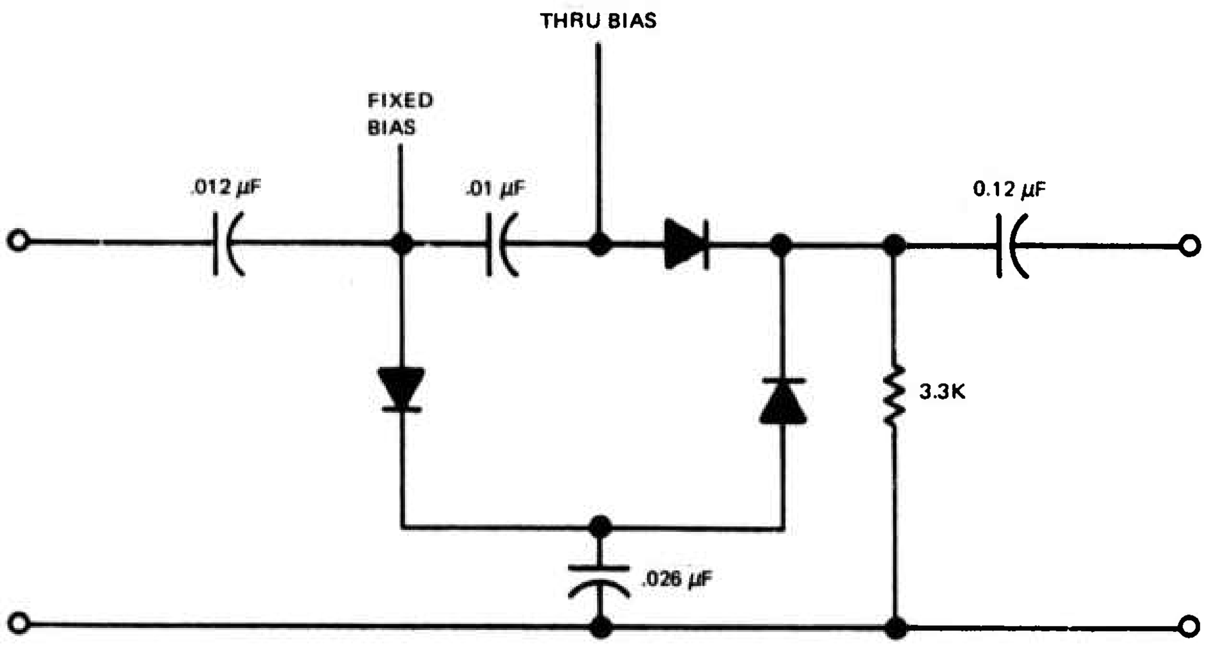


Figure 8.3-28. Attenuator Network.

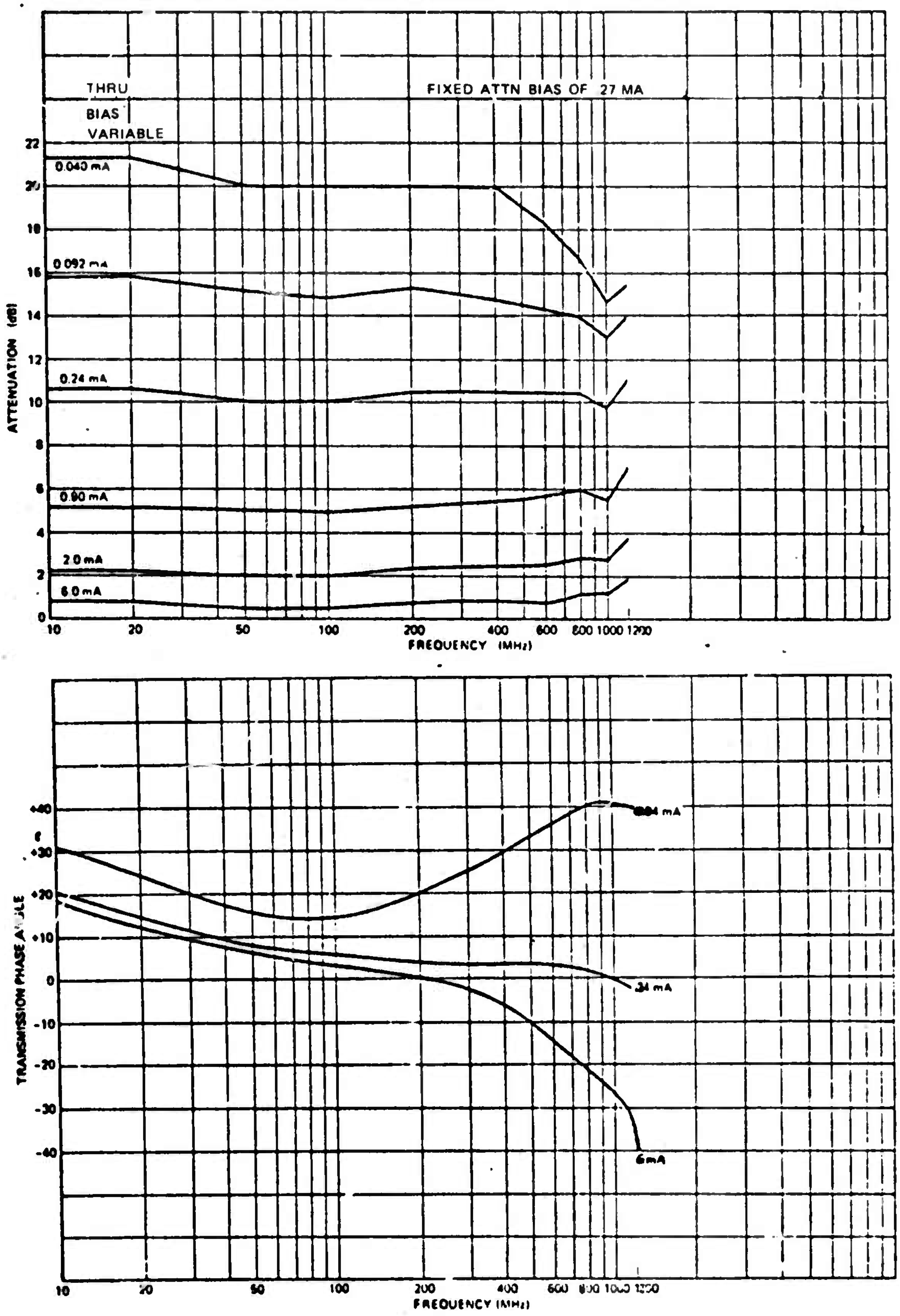


Figure 8.3-29. Attenuator Performance.

Table 8.3-4. Typical Amplifier Parameters.

PARAMETERS	AMPLIFIER			
	MIN	TYP	MAX	UNITS
Frequency Range	5	—	500	MHz
Gain	14	15.5	18	dB
Gain Flatness	—	± 0.25	±0.75	dB
Noise Figure (Note 2)	—	2.5	3.0	dB
Input and Output VSWR (50 Ω)	—	1.5:1	2:1	
Power Output, 1 dB Comp.	-2	0	—	dBm
3rd Order Intercept Point	—	+11	—	dBm
DC Supply Voltage	—	12	15	V
Supply Current (At +12 volts dc)	—	10	15	mA

The detected signal amplifiers tentatively selected are monolithic wideband dc amplifiers. These can be operated between +12- and -5-volt power levels. The device can provide between 10- to 20-dB gain in a 10- to 20-MHz range.

The store and hold circuit will be a diode gated or field affect transistor (FET) gated switch to a storage capacitor. At the end of preamble, the switch will be opened and the gain level that is stored on the capacitor will be held during the packet interval. The amplifier following the hold circuit represents additional gain to drive the attenuators and is a high impedance load on the storage capacitor.

A blanking input feature (used in optional multiple detectors) allows the same agc device to be used in expanding the radio with multiple detectors. The blanking input inhibits the peak detector and store circuits from detecting correlation peaks occurring in the blanking interval. The generation of the blanking signal is discussed in paragraph 8.3.4.10.

d. Packaging Data. The if. noncoherent agc amplifier will require approximately 13 square inches of printed circuit card area. This could be later reduced by using chips and packaging on a substrate. Since it has 45 dB of gain, it will be rf shielded from other units in the repeater or terminal.

The coherent agc amplifier consists of two 45-dB amplifiers packaged on a printed circuit card. Each is rf isolated from the other. Approximately 17 total square inches of surface area are required.

e. Control and Monitor. The control lines are identified in paragraph b., Functional Interfaces. A monitor output from the noncoherent agc amplifier is provided for test. For the coherent agc amplifier, the rf signal before detection will be available. The output of the attenuator driver will also be available to check time constants.

f. Power Estimates.

1. Noncoherent agc.

	+12 volts (mA)		-5 volts (mA)
RF Amplifier 1	10		
2	10		
3	10		
Detected Amplifier	8		4
Driver Amplifier	18		4
Misc Control	4		4
Total Current	62 mA		12 mA
Total Power	750 mW	+	60 mW = 810 mW

2. Coherent agc (Both Amplifiers).

	+12 volts (mA	-5 volts (mA)
RF Amplifier 1-1	10	
1-2	10	
1-3	10	
2-1	10	
2-2	10	
2-3	10	

3. Coherent AGC (Both Amplifiers).

	+12 volts (mA)	-5 volts (mA)
Detected Amplifier 1-1	8	4
2-1	8	4

	+12 volts (mA)		-5 volts (mA)
Driver Amplifier 1-1	18		4
2-1	18		4
Misc Control	20		4
Total Current	132 mA		20 mA
Total Power	1600 mW	+	100 mW = 1700 mW

8.3.4.10 Multiple Signal Processing

This paragraph of the equipment design plan describes the functions and operation of receive multiple signal processing. The fundamental purpose of multiple signal processing is to extract bit data from rf analog signals. Bit data detection may occur at two rates in repeater/station configurations. An option in these configurations is to extract multiple data streams occurring at a common data rate using common channels and common codes by using a feature of time discrimination unique to spread spectrum data communications.

Similar signal processing circuits are anticipated to meet the multiple processing needs. The signal processing must be capable of recovering data for the following.

a. 100 kBps - Terminal/repeater

b. 420 kBps - Repeater/repeater

c. 100 kBps - Multiple detectors - repeaters (optional)

d. 420 kBps - Multiple detectors - repeaters (optional)

Functionally, multiple signal processing is depicted in figure 8.3-30. Each signal processing, though similar in nature, performs data recovery for 100 kBps, 420 kBps, and multiple detection at these two rates. Note that for terminal operation, only one block is needed, the 100-kBps signal processing block. The switch logic is not required.

For repeater (and station) operation, the 100-kBps and 420-kBps blocks, along with a switch logic function are required. The switch logic connects either the 100-kBps or the 420-kBps interface functions to the microprocessor. Control of the rate switched is determined by which preamble arrived first.

For optional multiple detectors in repeaters and stations, the switch logic is not required.

Note that the multiple detectors can operate at either rate. The maximum number of detectors that can be used at 420 kBps is three, and 14 are possible at 100 kBps; however, the practical limit on the number of detectors is four. The multiple detectors do not contain SAWDs, but sample SAWD correlation outputs for identical code channels.

This paragraph on multiple signal processing is further subdivided in signal detection using SAWDs, preamble detection, bit sync acquisition, data detection, and use of the functions in multiple signal processing. The following elaborate on each of the areas.

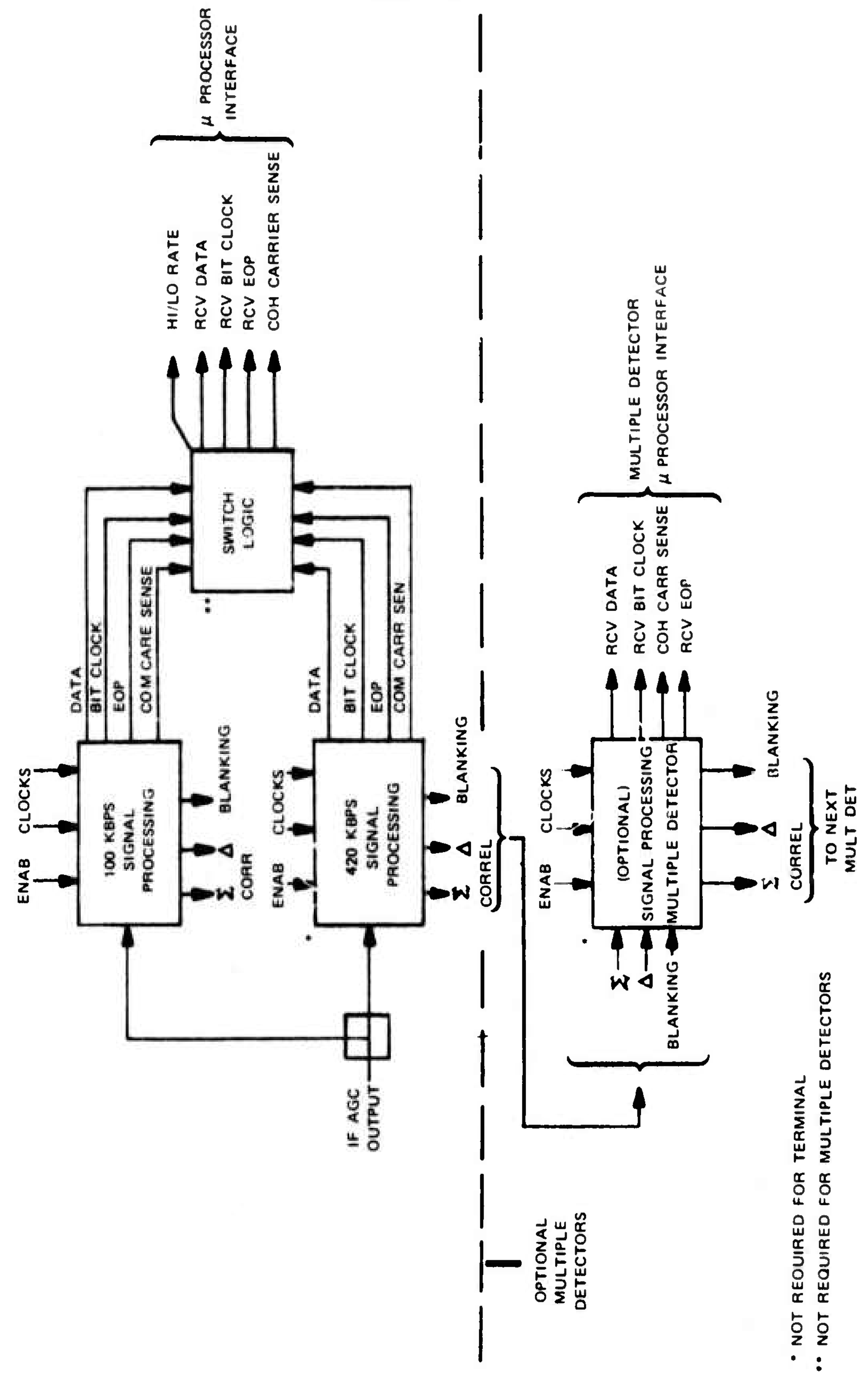


Figure 8.3-30. Multiple Signal Processing.

8.3.4.10.1 Signal Detection

a. Functional Description. A functional block diagram of the signal processing at the receiver is shown in figure 8.3-31. The differentially coherent msk demodulator consists of a SAWD with a cosine weighted input interdigital transducer spanning two chip intervals. The entire SAWD spans two bit intervals. It is a tapped delay line matched filter with the taps matched to the chips of two successive bits. The sum and difference of the bit outputs is envelope detected and applied to the preamble detector, the bit sync circuitry and the data detector.

b. Functional Interface. This functional interface pertains to a signal processing block (either 100 kBps or 420 kBps) as shown in figure 8.3-30. The top level multiple signal processing interface is the sum of 100-kBps and 420 kBps interface, plus optional multiple detector interfaces defined later.

IF Input	f_0 = 299.25 (± 0.020) MHz matched to other receive SAWDs and transmit SAWD to within ± 0.002 MHz Power = signal at -20 to -33 dBm. Level set by preceding noncoherent agc S/N ≥ -10 dB (E_b/N_o ≥ +11 dB) for 100 kBps ≥ -1 dB (E_b/N_o ≥ +11 dB) for 420 kBps
RCV Enab	COS-MOS logic level enabling receiver functions (agc set, preamble detection and and bit sync detection. These functions active only during preamble.)
Clocks	$4R_c$ (50.400 MHz) P_0 = 0 dBm
Data	Demodulated data at applicable bit rate. Data transitions synchronous with positive edge of bit clock.
Bit Clock	Rate at applicable bit rate, either 100 kBps or 420 kBps. Phase changes occur only between RCV Enable and End of Preamble.
End of Preamble	Signal detection of packet. Occurs at End of Preamble and start of data transfer.
Coherent Carrier Sense	Detection of signal above threshold. Signal may be desired signal, or interfering signal 20 dB higher.

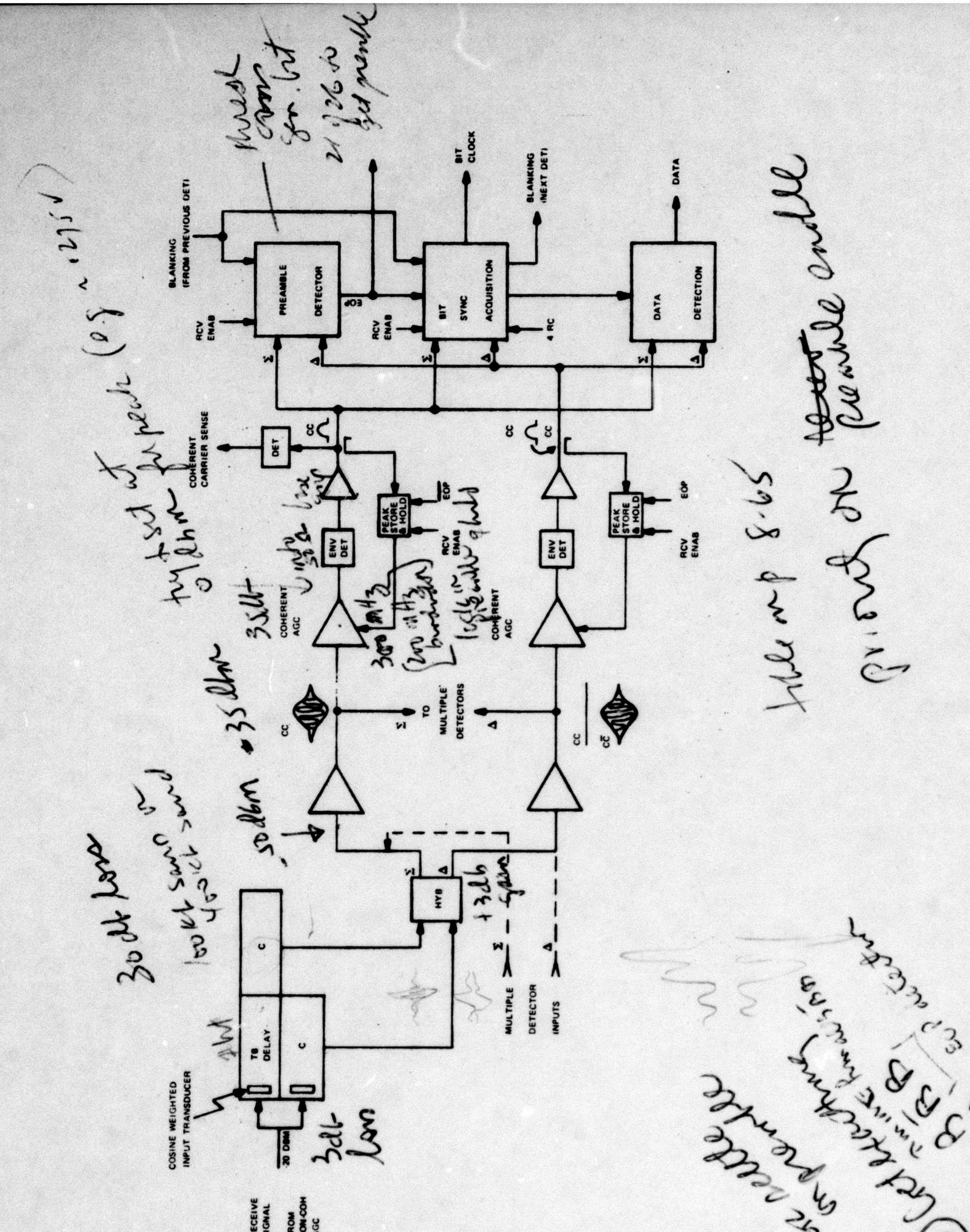


Figure 8.3-31. Signal Processing.

Blanking	Timing output to next multiple detector signifying time intervals where other packets are being processed.
Σ and Δ Correlations	Outputs from SAWD matched filter through hybrid combiner and amplified for use by following multiple detectors.

c. Design and Performance Analysis.

SAWD Matched Filter Detector

For the low rate mode the differentially coherent msk detector consists of a 20-μs surface acoustic wave device (SAWD) spanning a 2-bit interval. For the high rate mode, the SAWD length is 4.76 μs. The details of this SAWD detector are shown in figures 8.3-32 and 8.3-33. The input interdigital transducer to the SAWD is cosine weighted (-90 degrees to +90 degrees of the cosine waveform) with a duration of two chip periods or 0.159 μs. It is matched to the transmit SAWD as discussed in paragraph 8.3.4.1. The remainder of the SAWD is a nondispersive tapped delay line matched filter with the taps matched to the 252 chips corresponding to the successive bits. The 126 taps in each 10-μs section of the SAWD for the low rate mode are coded with the identical maximal length code sequence as discussed in paragraph 8.3.4.1. The even taps are summed, thus matching to one msk subchannel, and the odd taps are summed providing the match to the other subchannel. The carrier phase of one subchannel is phase shifted 90 degrees relative to the other subchannel. The two outputs are summed, yielding the match to the received signal. Each 126-chip SAWD filter can be represented by:

$$s(t) = (\cos w_o t) \sum_{k=0}^{62} d_{2k+1} \operatorname{cosp} \frac{\pi}{2T}(t - 2kT)$$

$$\sin w_o t \sum_{k=10}^{62} d_{2k+2} \operatorname{sinp} \frac{\pi}{2T}(t - 2kT)$$

Where cosine pulse cosp is defined by:

$$\operatorname{cosp} \frac{\pi t}{2T} = \cos \frac{\pi t}{2T}[u(t + T) - u(t - T)]$$

and sinp is defined by:

$$\operatorname{sinp} \frac{\pi t}{2T} \quad u(t) - u(t - 2T)$$

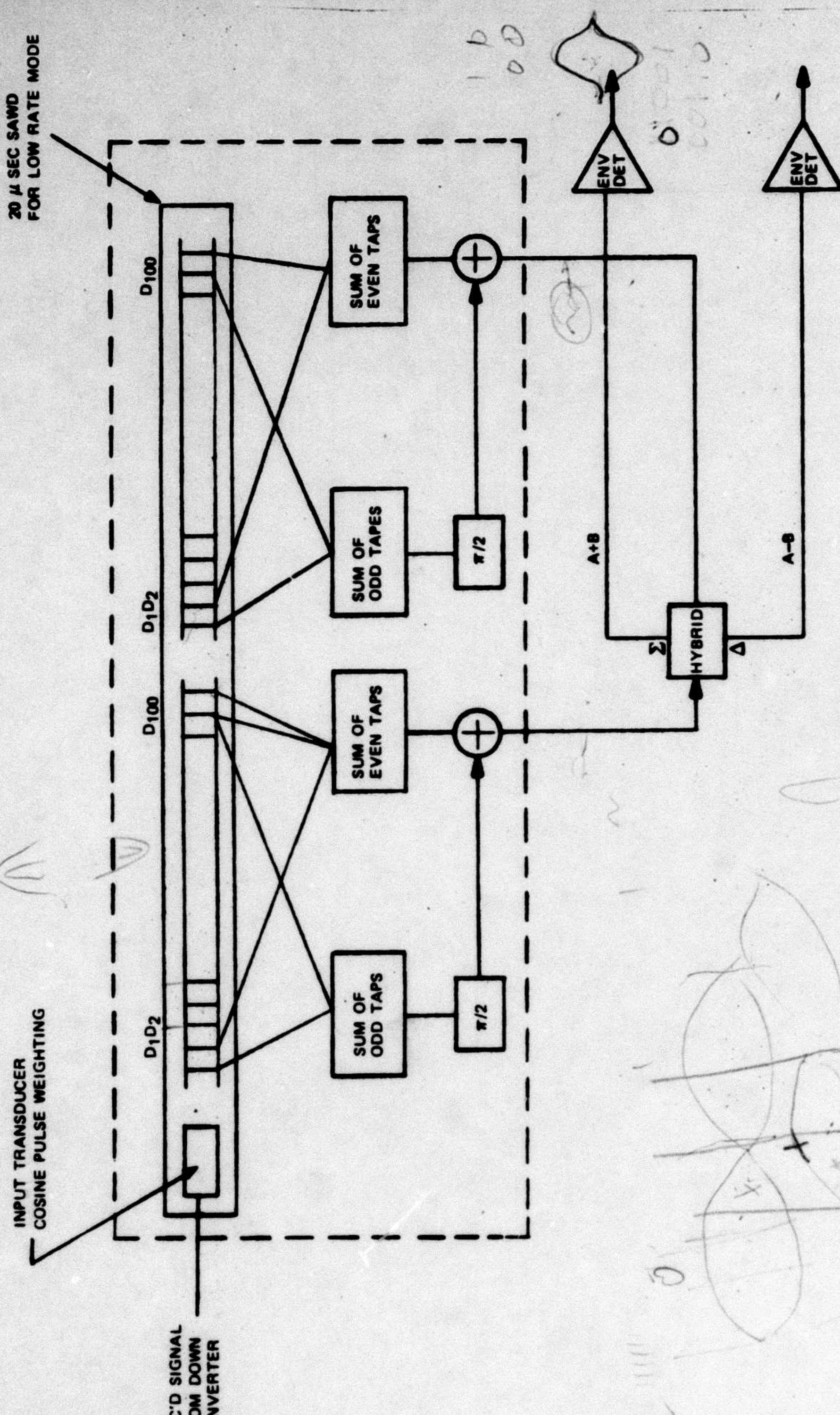


Figure 8.3-32. Differentially Coherent MSK Demodulator.

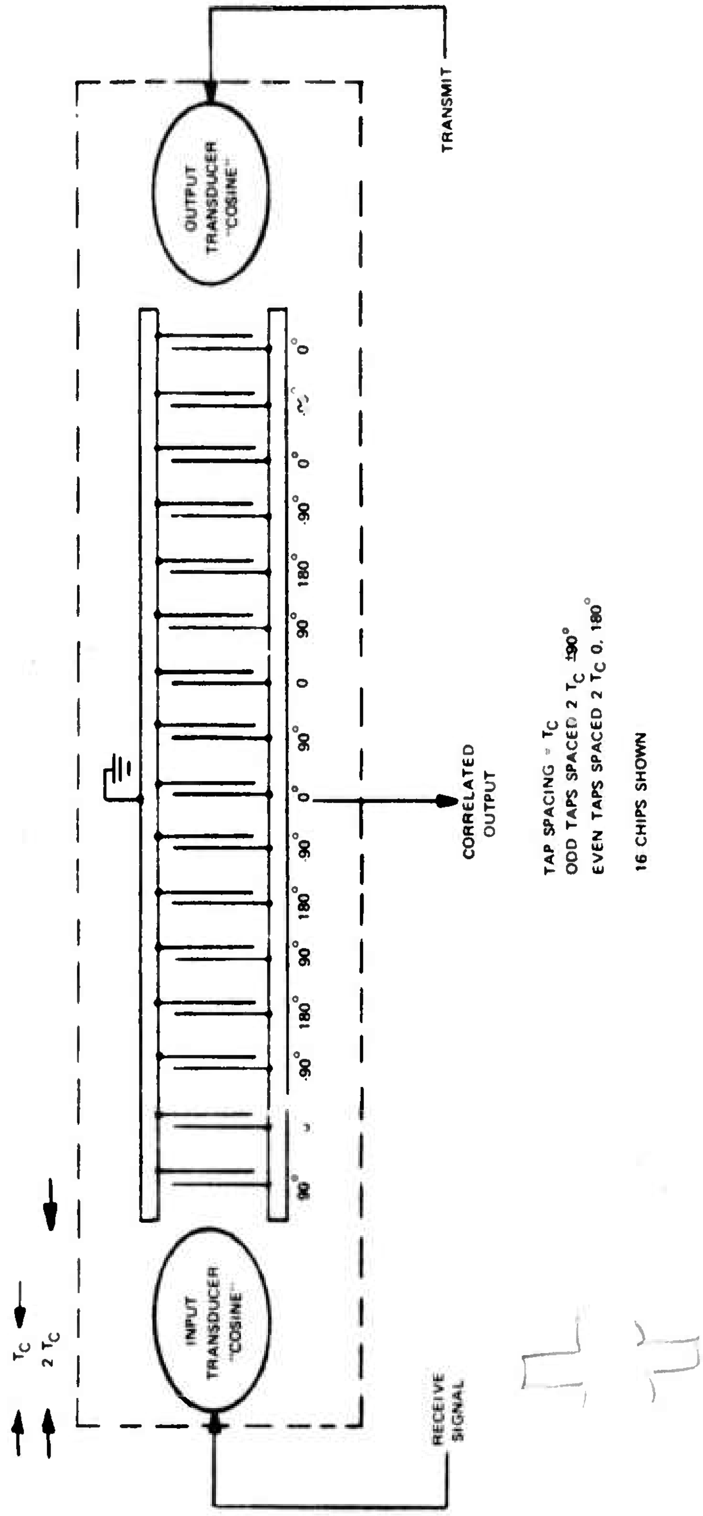


Figure 8.3-33. SAWD Implementation for MSK.

The center frequency of the SAWD is $w_o/2\pi$ = 299.25 MHz. The chip interval T is 0.0794 μs and u(t) is the unit step function. The decorrelated outputs A and B from the incoming bit and the delayed bit are input in a hybrid, which yields a sum and difference output. These two outputs are envelope detected and transferred to the preamble detector, bit timing recovery circuitry, and the data detector.

A theoretical performance curve of the differentially encoded msk signaling in an additive white Gaussian noise environment is shown in figure 8.3-34. The bit error rate is plotted versus the signal-to-noise ratio. The curves assumes ideal bit timing.

The effect of bit timing errors upon the loss of signal energy is shown in figure 8.3-35. For msk signals the correlation function is given by:

$$
\begin{aligned}
R(\tau) &= 2\cos\left(\frac{\pi t}{2T}\right) * \cos\left(\frac{\pi t}{2T}\right) \\
&= 1/2\left\{\cos\left[\frac{\pi(2T-|\tau|)}{2T}\right]\right\}\left[|\tau| - \frac{T}{\pi}\sin\left(\frac{\pi|\tau|}{T}\right)\right] \\
&\quad - \frac{T}{2\pi}\left\{\sin\left[\frac{\pi(2T-|\tau|)}{2T}\right]\right\}\left[\cos\left(\frac{\pi|\tau|}{T}\right) - 1\right]
\end{aligned}
$$

where τ is the timing offset and 1/T is the chip rate.

Independent coherent agc amplifiers are used in each hybrid output: one for Σ output and one for Δ output. Coherent agc is discussed in paragraph 8.3.4.9. A pickoff point preceding the coherent agc amplifier is used for Σ and Δ signal distribution to multiple detectors, if used.

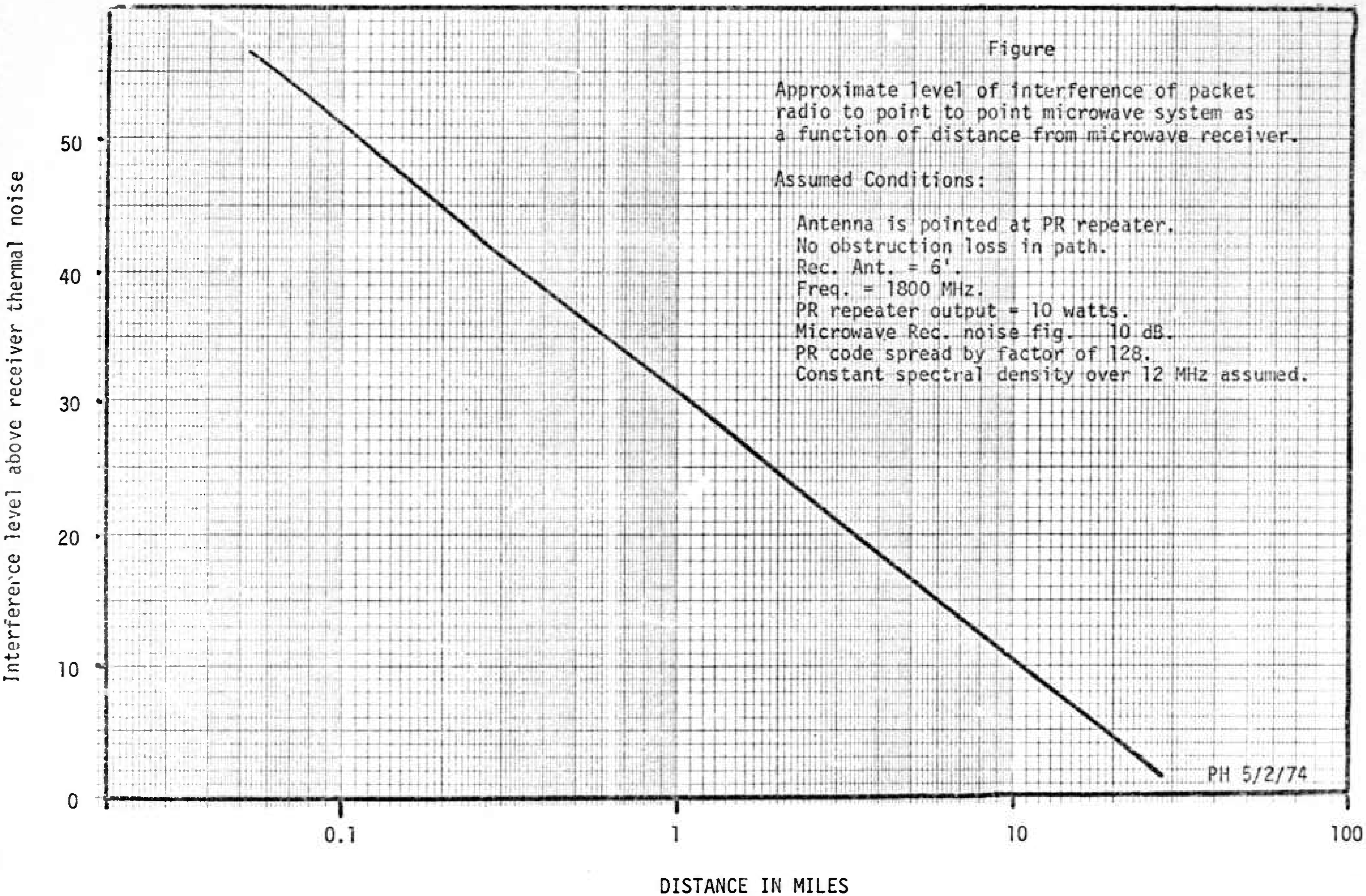
The baseband outputs from the envelope detector coherent agc circuits are fixed in level during the first 13 bits of preamble. The outputs are positive going only, ideally one correlation peak on one output (for example, Δ) with no pulse on the others (Σ output). These baseband correlation peaks are distributed to the three circuit blocks shown on the right in figure 8.3-31. Each of the blocks is shown in more detail in figures 8.3-36 through 8.3-38, and discussed in the following subparagraphs.

d. Packaging Data. Shielded modules requiring approximately 30 in.^{2} of printed circuit board area.

e. Control and Monitor. None.

f. Power Estimate. 1000 MW.

g. Additional Features. None.

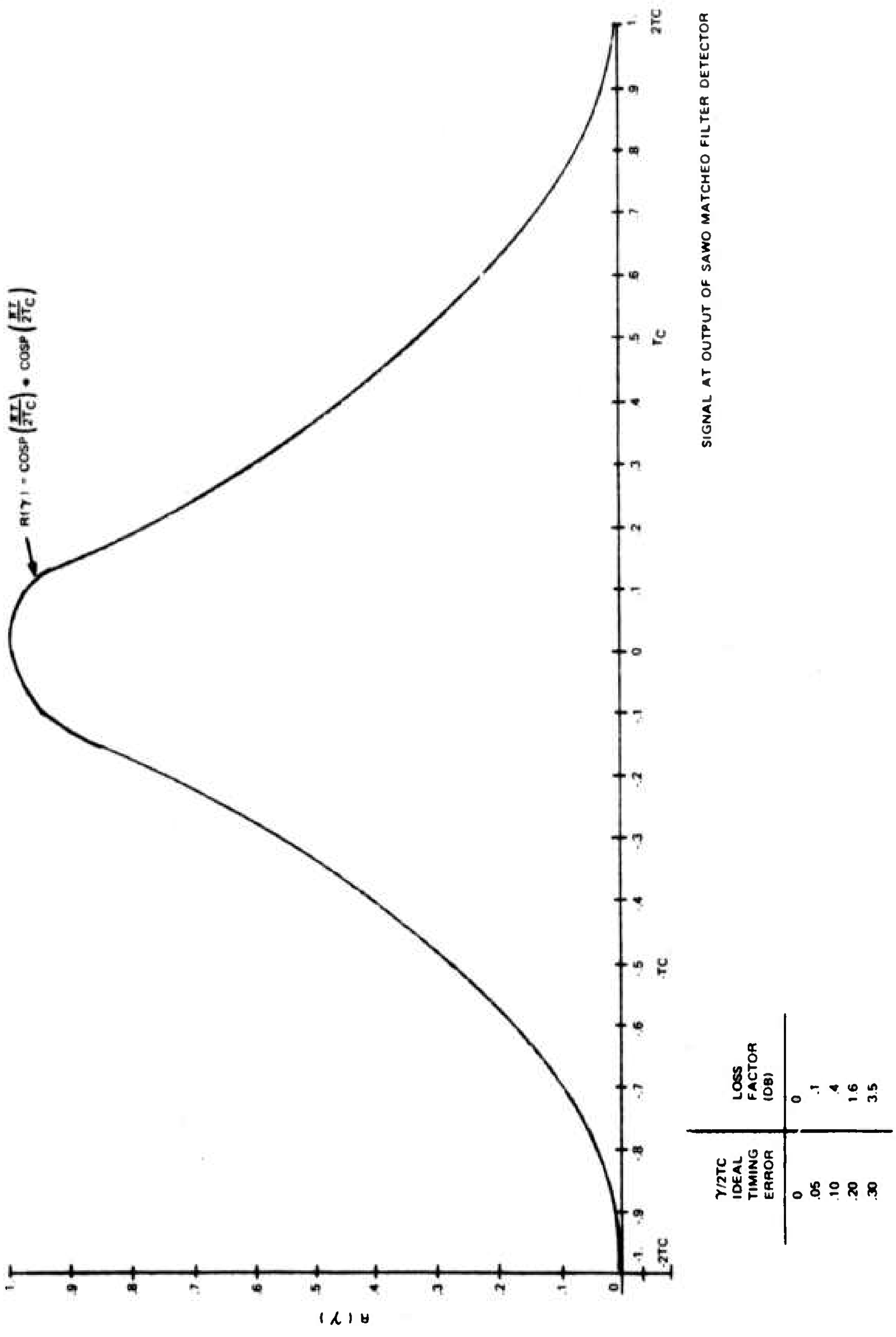


Figure

Approximate level of interference of packet radio to point to point microwave system as a function of distance from microwave receiver.

Assumed Conditions:

Antenna is pointed at PR repeater.
No obstruction loss in path.
Rec. Ant. = 6'.
Freq. = 1800 MHz.
PR repeater output = 10 watts.
Microwave Rec. noise fig. 10 dB.
PR code spread by factor of 128.
Constant spectral density over 12 MHz assumed.



γ/2TC IDEAL TIMING ERROR	LOSS FACTOR (DB)
0	0
.05	.1
.10	.4
.20	1.6
.30	3.5

Figure 8.3-35. Effect of Timing Offsets for Ideal Sampling of MSK.

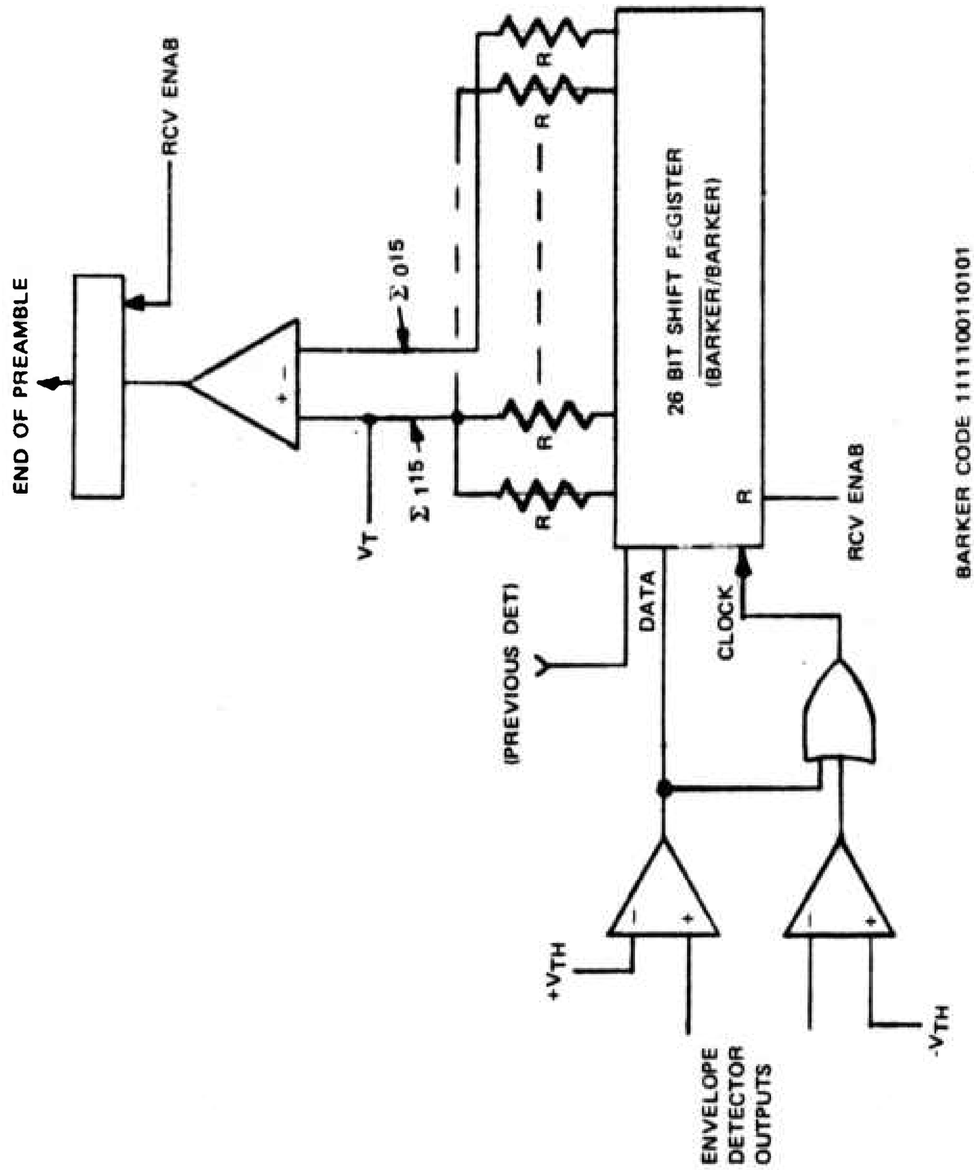


Figure 8.3-36. End of Preamble Detection (Asynchronous).

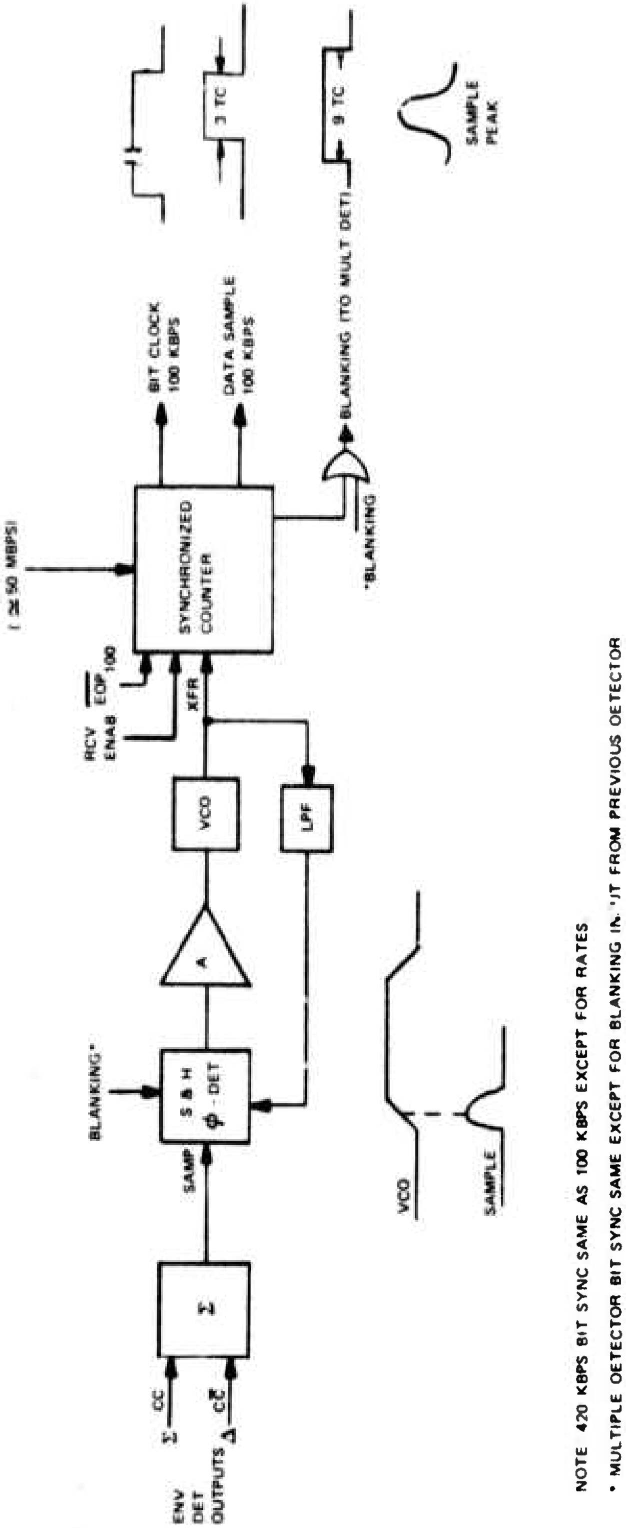


Figure 8.3-37. Bit Synchronization.

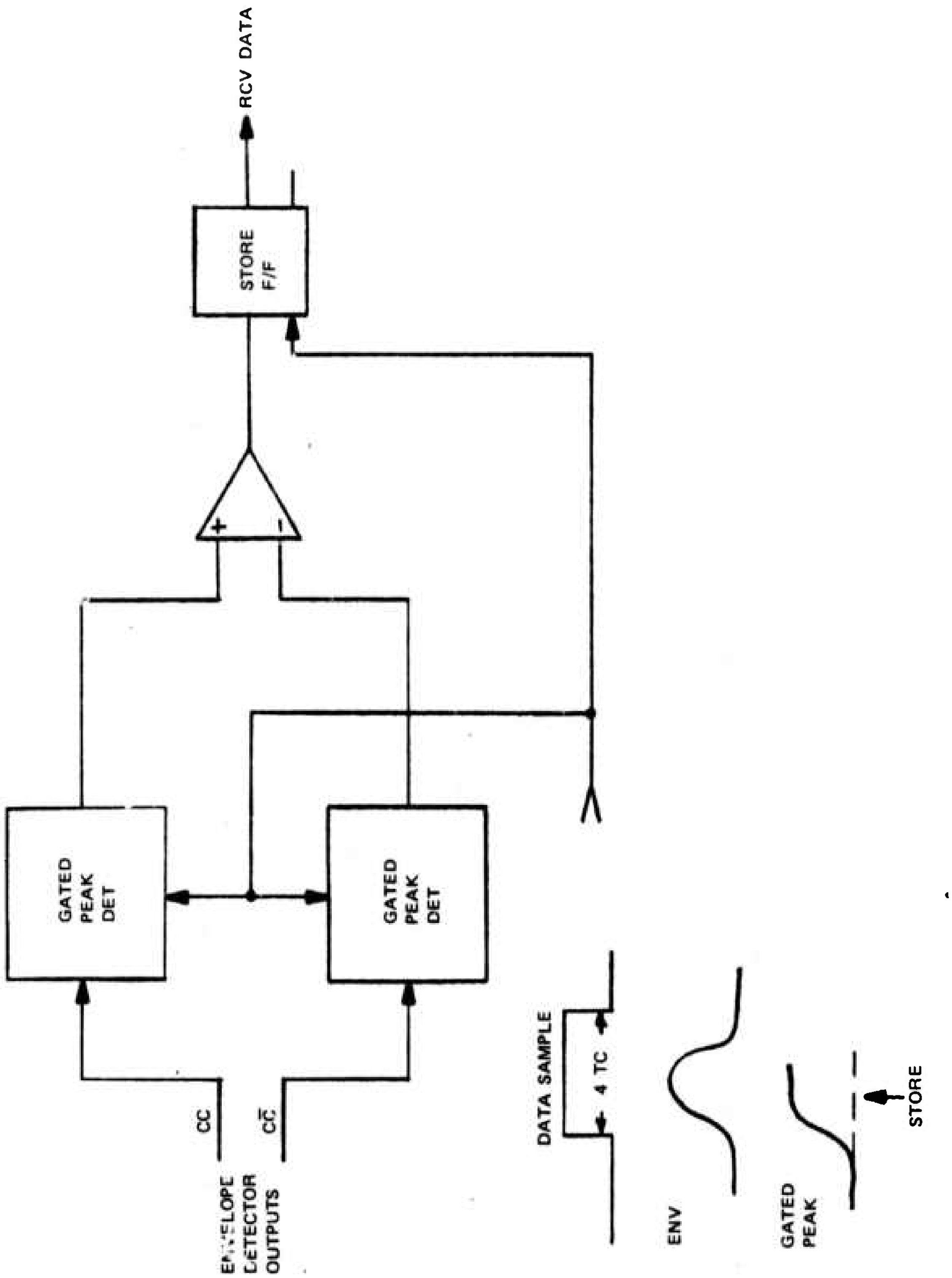


Figure 8.3-38. Data Detection.

8.3.4.10.2 End of Preamble

a. Functional Description. End of Preamble (EOP) functions to determine the end of preamble of a processed received packet and signals the start of data. EOP sets coherent agc to a hold state, disables bit sync acquisition (clocks allowed to free run), and informs the microprocessor of start of data.

b. Functional Interface.

Σ and Δ Baseband	Receive packet inputs from SAWD detectors for EOP processing. Approximately 1-volt peak level.
Blanking	Input from previous multiple detector signaling prior packet sampling intervals.
RCV Enable	EOP detection enabling function.
EOP Output	Detection of end of preamble/start data.

c. Design and Performance Analysis. The preamble detection implementation is shown in figure 8.3-36. In essence, the detector is a digital transversal filter matched to the 26-bit Barker, Barker sequence. The envelope detector outputs at points Σ and Δ of figure 8.3-31 are rounded pulses of 200-ns duration occurring at the bit rate. A pulse at Σ corresponds to a logic 1 and a pulse at Δ corresponds to a logic 0. A positive pulse at Σ exceeding the threshold yields an output pulse which is shifted asynchronously into the register. If the pulse at Δ exceeds the threshold, no pulse is shifted into the register, but the contents of the register are shifted right. The output taps of the register corresponding to the 1's in the Barker, Barker sequence are summed and similarly the 0's are summed. The difference of the sum is compared to a threshold, and when the threshold is exceeded, the end of the preamble is indicated. If the register initially contains all 1's and the 39-bit Barker, Barker, Barker preamble code is re- is received, the sequence of values at the output of the comparator (assuming that no errors occurred) is:

-2, -2, -4, -4, -6, -4, -4, -4, -6, -4, -6, -4, -18
-4, -6, -4, -6, -4, -4, -4, -6, -4, -4, -2, -2, 0
2, 0, 2, 0, 2, 0, 2, 0, 2, 0, 2, 0, 26
-1, 2, -1, 2, -1, 2, -1, 2, -1, 2, -1, 2, -13
0, -1, 0, -1, ---------------------------, EOP

The probability of a false alarm and the probability of a missed preamble is plotted in figure 8.3-39 as a function of the comparator threshold. The probability of a missed preamble as a function of the signal-to-noise ratio and is plotted for an SNR of 7.5 dB and 6.5 dB.

If the threshold is set to 21 out of 26, the probability of a false alarm is 10^{-7}. The probability of a missed preamble is 10^{-3} for a 6.5 dB SNR.

d. Packaging Data. 14 in.^{2} of printed circuit board area.

e. Control and Monitor. None.

f. Power Estimate. 330 MW.

g. Additional Features. Identical for terminal, repeater, and station.

8.3.4.10.3 Bit Sync

a. Functional Description. The purpose of bit synch is to align data sampling pulses with the received bits. Bit sync is used only during preamble. During preamble, phase of bit timing is transferred to a counter being clocked in 20-ns increments. After preamble, phase transfer is disabled, and timing is allowed to free run from a 20-ns clock derived from a stable frequency standard. This allows time discrimination for possible multiple packet use.

b. Functional Interface.

Σ and Δ Baseband	Receive packet inputs from SAWD detectors for bit timing acquisition.
RCV Enable	Enables bit timing acquisition during preamble.
EOP	Disables bit timing acquisition and transfers timing and information to a stable clock countdown.
Clock	4Rc (50.400 MHz) stable clock.
Bit Clock	Bit rate clock output to correlation peak. Phase change only during preamble search.
Data Sample	$3T_c$ sampling pulses (windows) for data sampling.
Blanking Input	Input from previous detectors in multiple detector use signaling packet processing intervals.

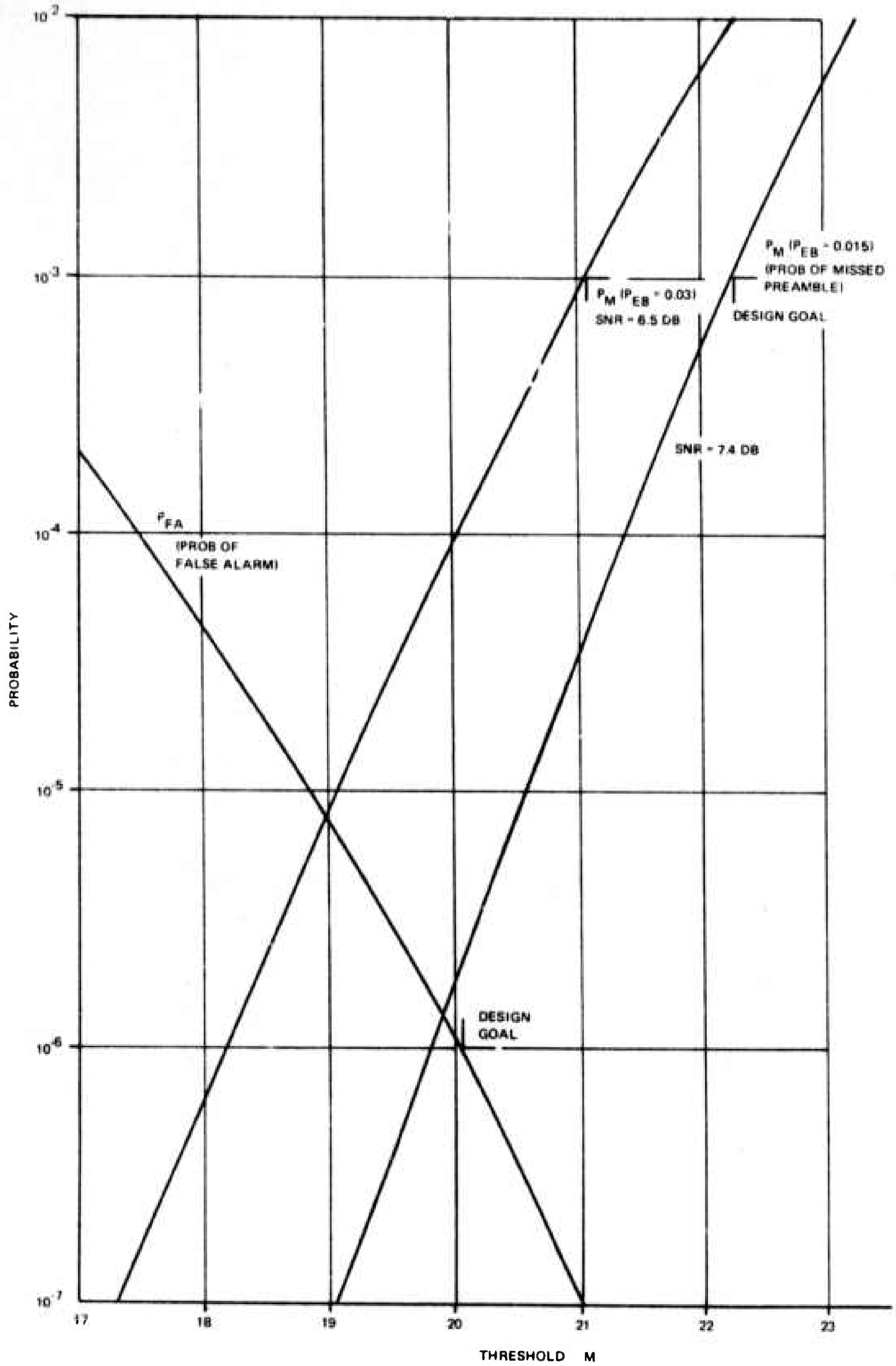


Figure 8.3-39. End of Preamble Detector.

Blanking Output	Output for multiple detector use signaling packet correlation intervals ($9T_c$ each) being processed.

c. Design and Performance Analysis. Refer to paragraph 8.3.4.7, Frequency Generation, for clock stability requirements.

Bit timing recovery is accomplished by the phase-lock loop shown in figure 8.3-37. A VCO is phase locked to the incoming envelope detected correlation peaks that occur at the bit rate. The correlation peaks sample the phase of the local 100-kHz reference in the low data rate mode, and 420-kHz reference in the high data rate mode. The sample and hold output is filtered and its output is the control voltage of the VCO. The VCO output is filtered to establish the phase detector characteristic as shown in the figure. After the VCO is locked to the correlation peaks (i.e., the zero crossing of the low-pass filter output occurs at the sample time), its timing is transferred to a counter derived from a stable clock. At the end of the preamble, the counter is no longer controlled by the VCO, but free runs for the duration of the packet.

Assume for the loop that $W_n = 2\pi\ 16$ kHz, $t = 1$, and a 100-kHz local reference. Then, with no noise, 2-bit times (20 μs) are required for frequency lock and an additional 70 μs are required to achieve a phase error of 1 degree or 28 ns. This assumes that the agc has been set.

Step response must be within 20 ns of final phase within 39 bit periods. Using f_N PLL bandwidth of approximately 16 kHz, 11 bits is sufficient for a high signal-to-noise environment. See paragraph 3.6 of appendix C.2 on synchronization preamble.

d. Packaging Data. 20 in.^{2} of printed circuit board area.

e. Control and Monitor. Out-of-lock output.

f. Power Estimate. 765 mW.

g. Additional Features Identical for all terminals/repeaters and stations except for 100-kBps and 400-kBps bit rates.

8.3.4.10.4 Data Detection

a. Functional Description. Purpose is to translate analog signals to digital data.

b. Functional Interface.

Σ and Δ Baseband	Receive packet inputs from SAWD detectors for data processing.
Data Samples	Pulse samples $3T_c$ in width from bit timing.
Data Output	Detected bit data to microprocessor.

c. Design and Performance Analysis. The method for data detection is illustrated in figure 8.3-38. It is achieved by sampling the SAWD matched filter output by a timing window that is $3T_c$ second wide where T_c is the chip interval, storing the peak value during that timing window, and making a bit decision at the end of the timing window. The decision is based on the difference between the two peak detected outputs. It is estimated that this form of detection degrades performance by 0.5 dB from the ideal timing case. Hence, performance of DCMSK with $P_e = 10^{-5}$ requires an $E_b/N_o = 10.9$ dB rather than 10.4 dB.

d. Packaging Data. 8 in.^{2} of printed circuit board area.

e. Control and Monitor. None.

f. Power Estimate. 460 MW.

g. Additional Features. Identical for all terminal, repeater, and station configurations.

8.3.4.10.5 Multiple Detectors

a. Functional Description. Detects packet data in the presence of other packets. Multiple detectors use SAWD detector outputs (same data rate) of primary detectors. Figure 8.3-30 is a functional view of how the multiple detector is used.

Note that multiple detectors may be either data rate. Detectors may be extended to a maximum of three at 420 kBps and to a practical limit of four at 100 kBps.

b. Functional Interface. This functional interface for multiple detectors is in conjunction with the signal processing interface described earlier.

Σ and Δ Correlations	Outputs from SAWD detectors from primary detectors.
RCV Enable	Enables receiver operation.
Clock	4Rc (50.400 MHz) stable clock.
Data	Same as signal processing.
Bit Timing	Same as signal processing.
EOP	Same as signal processing.
COH. CARR Sense	Same as signal processing.
Blanking Signal	Same as signal processing.

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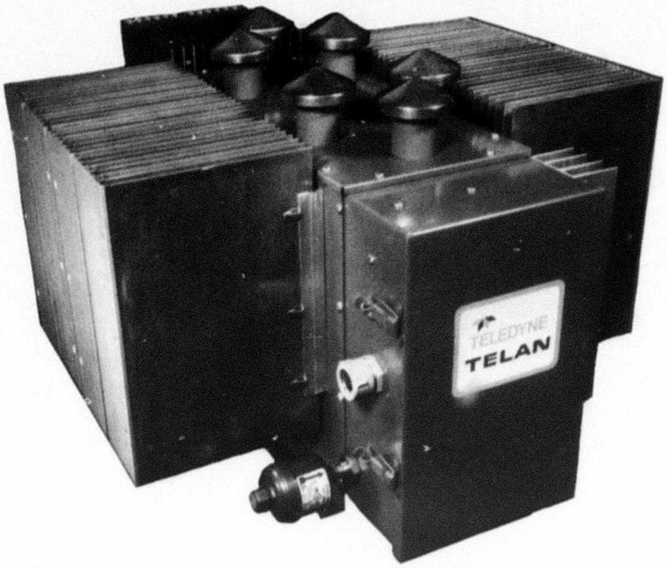

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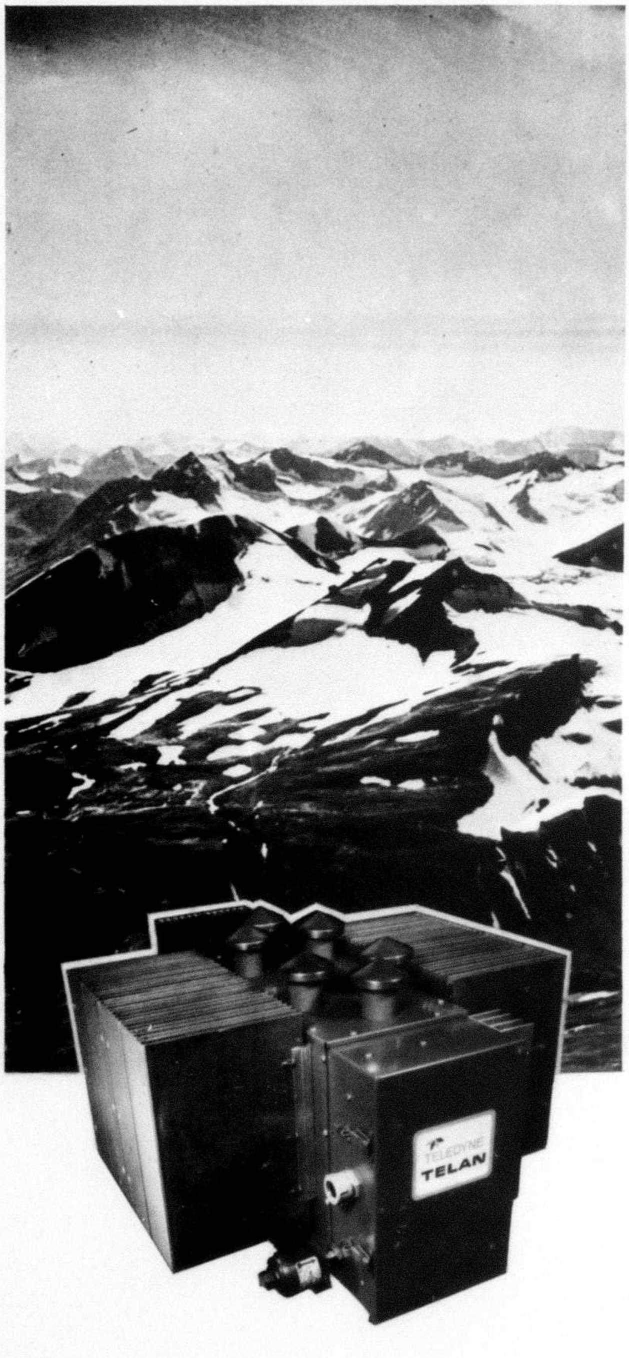

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TELAN Thermoelectric Generators are the most reliable and most economical source of electrical power to meet the needs of equipment installed in remote locations. They eliminate the need for batteries and battery replacement, or for engine-driven generators.

Completely weatherproof, TELAN generators convert heat from the flameless combustion of propane, butane or natural gas, directly into electrical energy without risk or hazard. They are highly reliable, long duration sources of electrical power (as high as 90-watts in a single unit), with a minimum of service required. In comparison with other forms of electrical power, TELAN Thermoelectric Generators are favored economically over batteries where the requirement is for more than 1-watt, and over engine-driven generators where the electrical power requirement is less than 300-watts. Almost invariably, the economics of using TELAN are significant compared to construction of power lines which can cost $10,000 per mile depending upon terrain.

TELAN® Thermoelectric Generators should be your first choice for electricity when:

- Reliability is the prime consideration
- Power levels are 8 watts or larger.
- The location is remote and access is difficult
- Power is required for at least 3 months
- Continuous, unattended power is required

advantages of TELAN® thermoelectric generators

ECONOMY

No other form of providing electricity compares to TELAN for economy within its power range. Operating costs can be figured at $3.60 per watt-year for average power consumption. Maintenance costs are negligible.

RELIABILITY

TELAN generators will go on year after year providing reliable power without maintenance, service, or repair. Periodic refueling is all that is necessary to keep TELAN generators operating.

SAFETY

Flameless operation greatly reduces any hazard to fuel supplies, personnel, or associated equipment. Burner Temperature Regulation reduces problems caused by malicious tampering, changes in heat value of the fuel, or accidental maladjustment.

NO MOVING PARTS — VIBRATIONLESS

All that moves is the fuel. There are no moving parts, no noise — and TELAN generators are so free of vibration that they will not disturb adjacent sensitive seismic instrumentation. No lubrication is needed . . . ever.

SIMPLE, FOOLPROOF OPERATION

TELAN units can be installed by inexperienced, non-technical personnel. In underdeveloped countries, local personnel can be utilized. Variations in fuel pressure and/or heating value are automatically accommodated and self-adjusted by the built-in temperature regulator, keeping heat input to any or all burners at a safe level at all times.

CAN BE OPERATED IN ALL WEATHER AND TEMPERATURES

TELAN generators are normally installed without enclosures — no special housing is needed. Weather and corrosion resistant materials are used throughout. Wind, rain and snow actually improve the performance of the units (see graph below). They are fully reliable at sub-zero temperatures of the Arctic, or at 150°F temperatures of the tropical desert. In extreme cold climates reject heat from units may be used in shelters to keep vital electronics warm

VERSATILE

TELAN generators can be supplied to operate on Propane, Butane, or natural gas. Jets can be changed in the field if the fuel is changed after installation.

PORTABLE

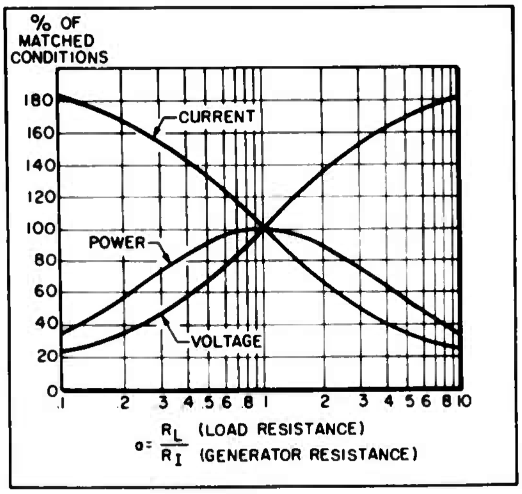
Small and relatively light in weight, TELAN generators are easily transported to any remote location.

MOUNT ANYWHERE

TELAN generators may be mounted on the ground, in or on a building, on a pole, tower, or tree . . . anyplace where it is most convenient.

CLEAN

Complete, flameless combustion of the gas results in no soot formation, no stacks or combustion chambers to clean, no hazard from accumulation of combustion by-products.



LOAD RESISTANCE

Illustrated is the relationship between current, power, and voltage at varying resistance loads. When the generator's internal resistance equals the load resistance, maximum power is delivered. This curve is typical for generators without the DC to DC converters.

EFFECT OF ENVIRONMENT

TELAN Thermoelectric Generators are designed and constructed for extreme dependability under all conditions. As shown here wind, rain and snow actually improve the performance of the generators. Heat generated for the production of electricity also keeps the unit snow and ice free in any weather. Power output is dependent on temperature difference between ambient and catalytic burner.

SPECIFICATIONS FOR TELAN THERMOELECTRIC GENERATORS

	Electrical Spec. (Minimums)			Std. Avail. Electric Outputs					Fuel Consumption		Size and Weight			
Generator Model	P W	E V	I A	Power Condition Code	Standard Wiring Code	P W	E V	I A	Propane Butane Lb./Wk. (Kilos/Wk)	Natural Gas MCF/Wk (M^3/Wk)	H In. (cm)	W In. (cm)	L In. (cm)	Wt. Lb. (Kilos)
Telan 2T1	10	4.8	2.1	12CL	10S	8	12	.67	11.2	.5	17	11	19	33
				24CL	10S	8	24	.33	(5.1)	(14.2)	(43)	(28)	(48)	(15)
				48CL	10S	8	48	.17						
Telan 2T2	20	9.6	2.1	12XL *	20S	19	12	1.58						
				12CL *	20S	17	12	1.41	22.4	.9	17	25	14	52
				24CL	20S	17	24	.71	(10.2)	(25.5)	(43)	(64)	(36)	(24)
				48CL	20S	17	48	.35						
Telan 2T3	30	14.4	2.1	12XL	30S	30	12	2.50	33.6	1.4	17	25	23	73
				24CL	30S	25	24	1.04	(15.3)	(39.7)	(43)	(64)	(58)	(33)
				48CL	30S	25	48	.52						
Telan 2T4	40	19.2	2.1	12XL	20S	40	12	3.34	44.8	1.9	17	25	22	93
				24XL	40S	40	24	1.67	(20.4)	(53.8)	(43)	(64)	(56)	(42)
				48CL	40S	34	48	.70						
Telan 2T5	50	24.0	2.1	12XL	25S	50	12	4.16	56.0	2.3	17	25	31	112
				24XL	50S	50	24	2.08	(25.4)	(65.2)	(43)	(64)	(79)	(51)
				48CL	50S	42	48	.87						
Telan 2T6	60	28.8	2.1	12XL	30S	60	12	5.00	67.2	2.8	17	25	30	130
				24XL	60S	60	24	2.50	(30.5)	(79.3)	(43)	(64)	(76)	(59)
				48CL	60S	51	48	1.06						
Telan 2T7	70	33.6	2.1	12XL	35S	70	12	5.82	78.4	3.3	17	25	39	149
				24XL	70S	70	24	2.91	(35.6)	(93.5)	(43)	(64)	(99)	(68)
				48CL	70S	59	48	1.23						
Telan 2T8	80	38.4	2.1	12XL	20S	80	12	6.65	89.6	3.7	17	25	38	170
				24XL	40S	80	24	3.33	(40.7)	(104.8)	(43)	(64)	(97)	(77)
				48XL	80S	80	48	1.61						
Telan 2T9	90	43.2	2.1	12XL	30S	90	12	7.50	100.8	4.2	17	25	47	189
				24XL	45S	90	24	3.76	(45.8)	(119.0)	(43)	(64)	(119)	(86)
				48XL	90S	90	48	1.88						

* For best efficiency, use the 2T2 12XL generator with load voltages below 13.8 VDC. Use the 12CL for voltages from 13.8 to 16 VDC.

(1) P indicates generator will be shipped with jets for Propane. Substitute "B" for Butane or "N" for Natural Gas jets. Jets can be changed in the field if fuel is changed after generator is installed.

(2) Warranty Power within ±5% at room temperature (70°F).

(3) Solid state DC–DC converter with variable voltage limiter, Specify 12, 24V, or 48V; variable range 12 to 16V, 24 to 31V and 48 to 56V. Code "CL". A slight drop in power will occur when operating at voltages other than rated voltage.

(4) Without DC–DC converter. Voltage limiter only — Code "XL".

(5) Kilos/week

(6) Cubic meters/week

- Shown are standard output voltages. Any other output voltage (for example, 76 volts) can be supplied. Contact factory for further information.
- The rectifiers in TELAN DC–DC converters prevent the battery from discharging into the generator. When a unit without converter is used to charge battery a blocking diode must be included to prevent battery discharge thru the TELAN unit.
- All generators include a gas regulator set to accept 10–30 psi: complete with weatherproof housing and weatherproof electrical convenience box.
- These units can be combined to satisfy larger power requirements. Contact our representative in your area or contact our factory for assistance.

"Prices and specifications contained in catalogs or advertisements of thermoelectric generators and ancillary equipment are subject to change without notice. The equipment advertised or quoted on by representatives of Isotopes, Inc. is covered by specific warranties on performance, materials and workmanship which establish a limit of obligation."

TELEDYNE ISOTOPES

110 W. Timonium Rd. Timonium, Md. 21093
PHONE: 301-252-8220 TELEX: 87-780

these features make TELAN® thermoelectric generators the first choice for reliable, unattended REMOTE POWER

HIGHER POWER OUTPUT

New improved TELAN Thermoelectric Generators provide over 10% more power output than previous units. This results in lower gas consumption per watt-hour, lower fuel costs, fewer refuelings, and longer lasting generators.

FLAMELESS — EXTREMELY STABLE THERMAL SOURCE

TELAN units operate by the catalytic burning of fuel. There is no flame to go out. Fuel or air flow can be interrupted for 3 minutes or longer depending on the ambient temperature and combustion will continue spontaneously when system is restored.

BURNER IGNITION

TELAN Thermoelectric Generators may be easily started with a match or cigarette lighter, or by means of an electrical igniter.

EXPLOSION PROOF DESIGN

Operating temperatures, by virtue of catalytic combustion, are about 600°F which is below the spontaneous combustion point of most explosive mixtures.

ALL SOLID-STATE PHYSICS — NO MOVING PARTS

The thermoelectric power generating modules are all highly reliable semiconductor devices.

COMPLETELY WEATHERPROOF HOUSING

Weatherproof, corrosion-resistant housing is standard for all TELAN Thermoelectric Generators.

SELECTION OF FUELS

TELAN units can be operated on propane, butane and natural gas.

CONTINUOUS POWER

TELAN Thermoelectric Generators produce power continuously. Unlike engine-driven power sources, they operate most efficiently in the continuous mode, and seldom require maintenance. Field reports verify some units have been operated for 4 years without maintenance.

MODULAR CONSTRUCTION

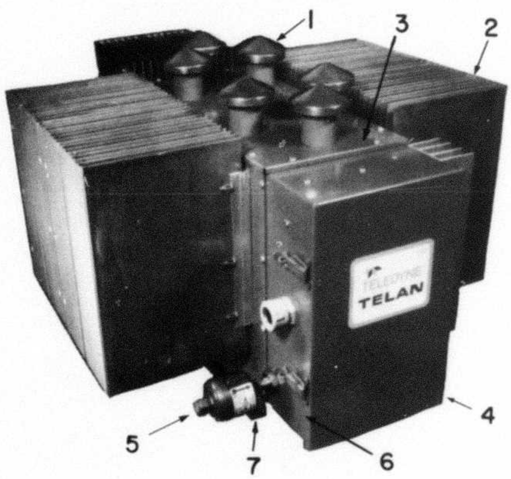
You need buy only as many identical power assemblies in single housings as required. You never buy more power than you need.

SIMPLE OPERATION

TELAN units can be installed and operated by unskilled personnel. Maintenance is very simple . . . no special training required.

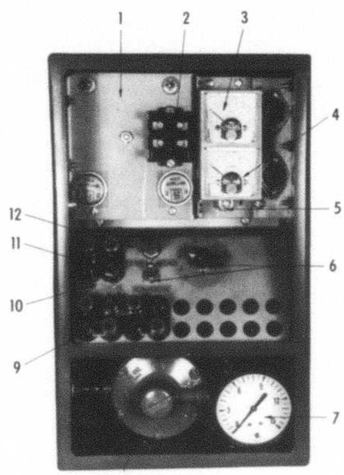
CUSTOM POWER CONDITIONING AVAILABLE

In addition to the standard output voltages of the TELAN units, any specific voltage level can be provided to meet individual requirements.



IMPORTANT EXTERNAL FEATURES

1. "COOLIE HATS" over intake and exhaust ducts (identical to prevent wind induced pressure differences) 2. Heat rejection fins 3. Weather-tight housing 4. Weather-tight electrical box (see Internal Features) 5. Gas connection (filter mounted externally) 6. Contains: Air intake plenum chamber, Gas manifolding and spuds, BTR valve, Electrical harnesses 7. Mounting base



IMPORTANT INTERNAL FEATURES
(inside weather-tight electrical box)

1. DC-DC converter* 2. Power output 3. Voltmeter* 4. Ammeter* 5. Variable voltage limiter* adjustment screw 6. Ignition switch* 7. Gas pressure gauge 8. Gas pressure regulator 9. Readily accessible test points for monitoring individual module performance 10. Convenient tie point for ignition power 11. Convenient tie point for alarm* 12. Thermocouple jack output for pyrometer

*Optional items

how TELAN® thermoelectric generators work

The basic theory behind operation of TELAN Thermoelectric Generators has been known for more than 150 years. This thermocouple effect, also known as the Seebeck effect, states that a voltage will be generated when one junction between two dissimilar metals is hotter than the other junction. Practical use of this property has been rapidly advancing over the past decade, and the application of modern semiconductor technology made possible one of the most efficient and economical electrical generators yet devised for relatively small amounts of power. This generated voltage is proportional to the temperature difference between the cold and the hot ends on the semiconductor thermoelectric material.

Heat in the TELAN thermoelectric Generator is supplied by the combustion of propane, butane, or natural gas; in a low temperature, catalytic process, which is extremely stable and safe, the noble catalyst bed remains active down to low temperatures (about 300°F) which is sufficient to burn the gas mixture. Combustion takes place in completely enclosed chambers with long intake and exhaust manifolds, as shown in the figure.

In the "n" leg of the thermocouple the excess electrons on the hot side will have higher kinetic energy than those on the cold side. Thus, the "hot" electrons will drift toward the cold side, carrying with them a negative charge. The cold end becomes negative relative to the hot end.

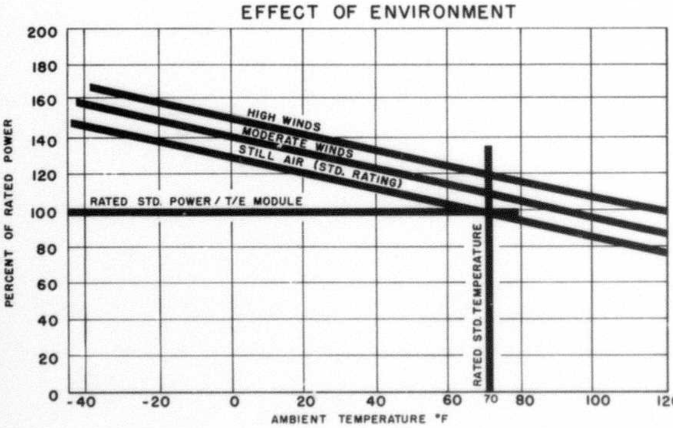
In the "p" leg the hole carriers will, in a similar manner, drift toward the cold side, imparting a positive charge. When a bus is connected across the two legs, the voltages add.

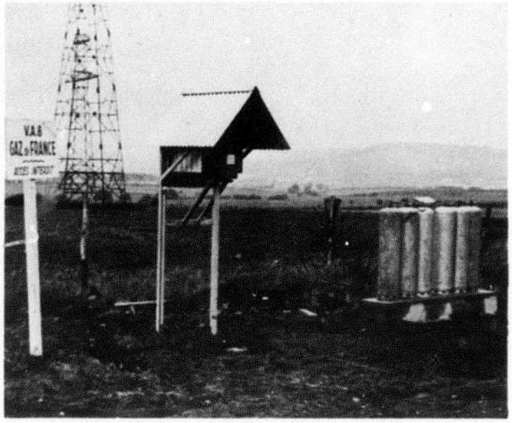
In a TELAN Thermoelectric Generator many such n and p legs are connected in series to give a more useful voltage from each thermoelectric module.

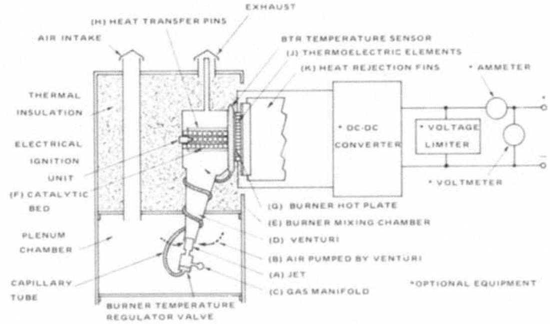
BUILT-IN "CIRCUIT BREAKER"

When current flows through a thermoelectric module in a TELAN generator, heat is pumped, according to the Peltier effect, in proportion to the current from the hot side to the cold side. This reduces the ΔT, which reduces the generated voltage, which in turn reduces the current. Thus, it is impossible to damage a thermoelectric module with an overload, and it can operate continuously with a short-circuited output. TELAN generators are also capable of operating continuously in open-circuit conditions.

EFFECT OF ENVIRONMENT







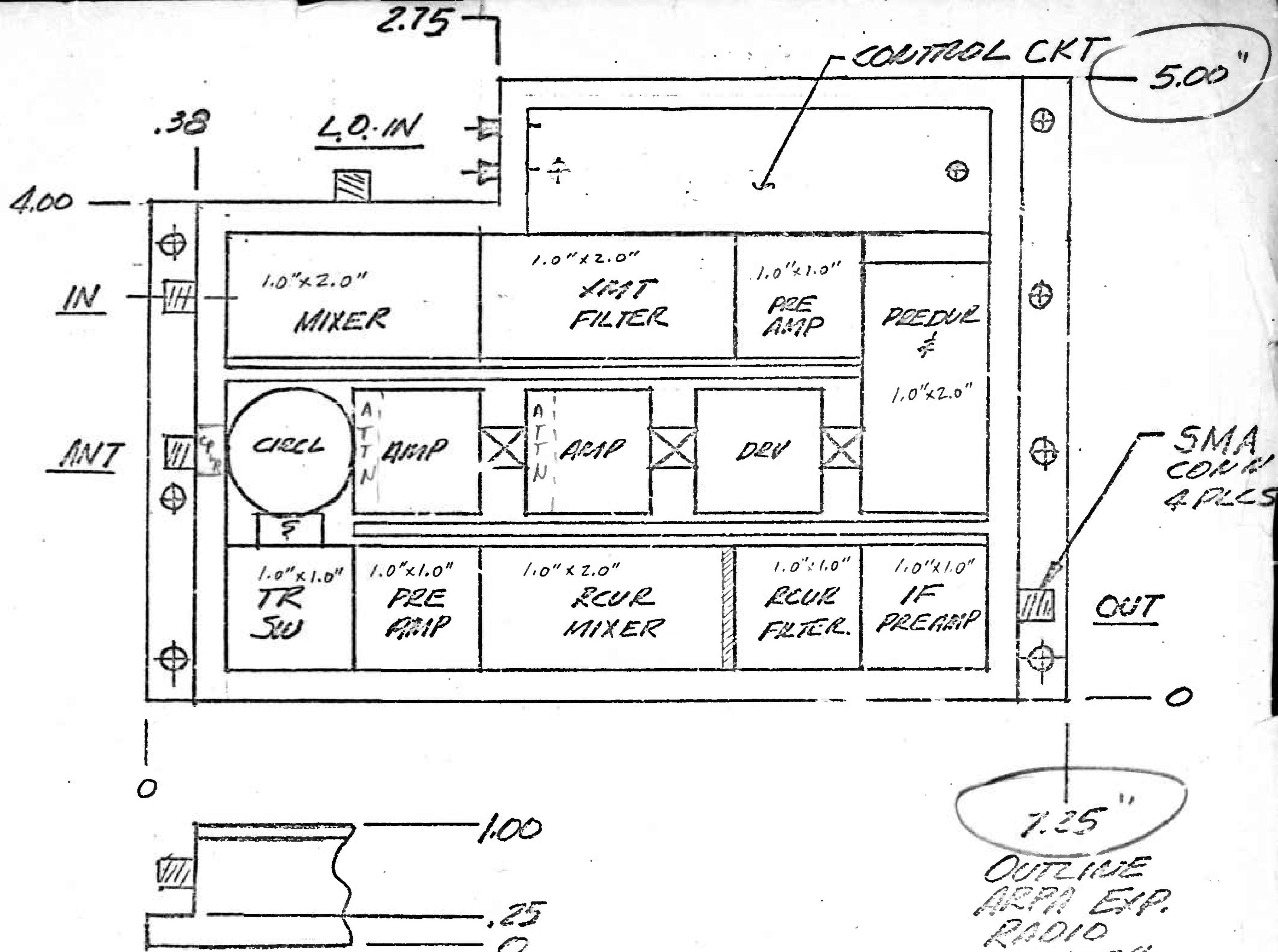
Flow of low pressure propane, butane or natural gas through jet (A) from intake manifold (C) ingests primary air (B) by venturi action (D). Air and gas enters totally enclosed mixing chamber (E) and impinge on catalytic bed (F) where low temperature oxidation and heat occur. The thermal energy is transferred to the hot plate of the burner (G) by heat transfer pins (H) located in the catalytic bed. The hot plate (G) raises the temperature of one side of the thermal element (J). The other side is cooled by the heat rejection fins (K).

TELAN® THERMOELECTRIC GENERATOR INSTALLATION

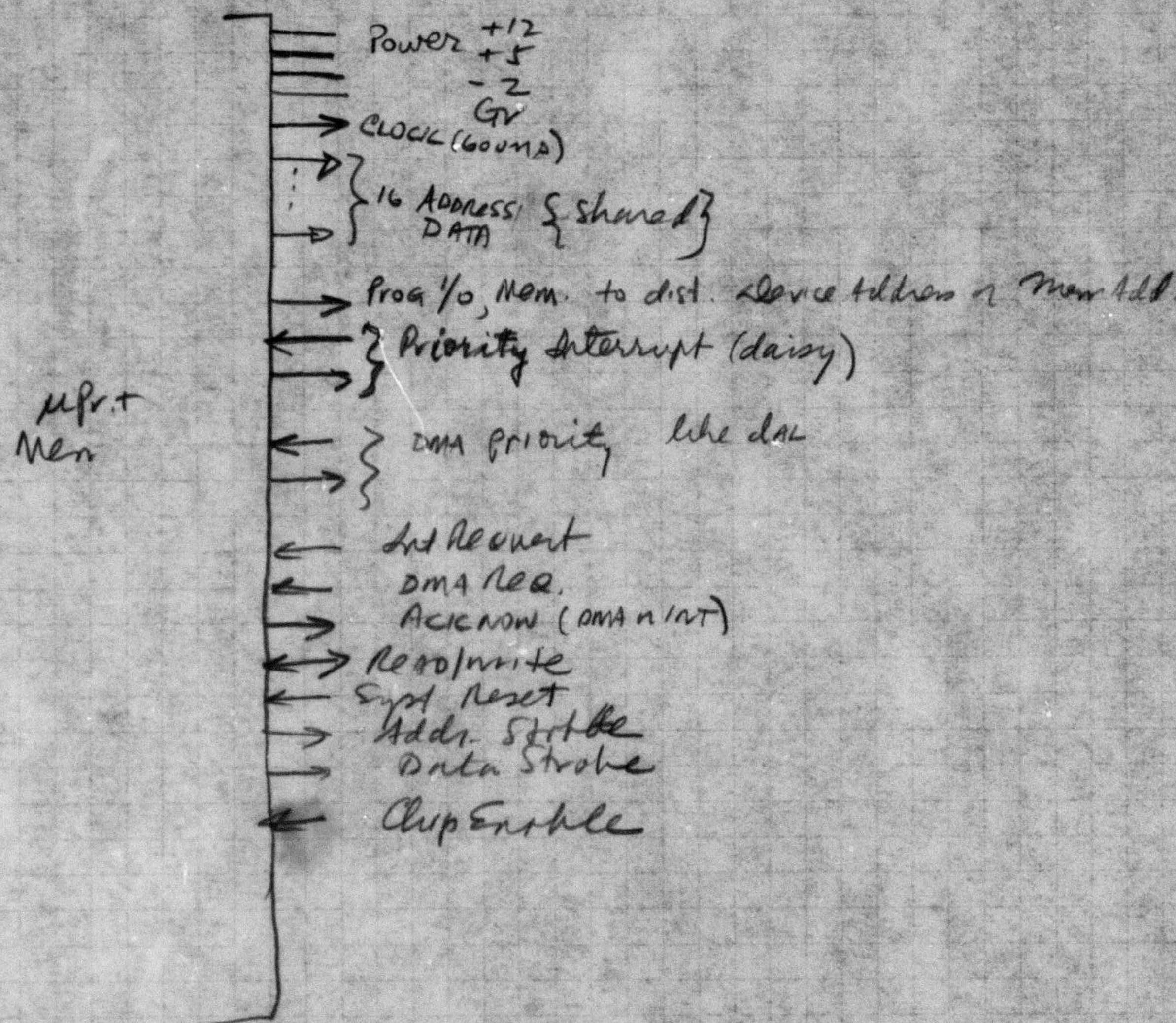
All TELAN Thermoelectric Generators are intended for use outdoors and require no additional housing. Since there are no moving parts, the mounting platform may be designed for static loads only. Generally a raised platform is preferred because it allows better cooling and protects from flooding in low-lying areas and heavy rains. Normal maximum temperature is 150°F. in still air but will be derated (see curve-Effect of Environment). Therefore, in hot environments that also have long periods of direct solar radiation heating, a sun shade may be advisable.

FUEL SUPPLY: Low temperature operation is limited only by fuel vaporization. Butane should be used only where temperature will not go below +35°F for long periods. If propane is to be used in environments below −35°F provisions should be made for keeping the gas supply warm such as using excess heat from the TELAN unit or burying the tank in the ground or snow.

ELECTRICAL CONNECTIONS: All electrical connections are made to screw terminals inside a weather-tight electrical convenience box mounted on the front of the TELAN unit. A weatherproof fitting is provided to seal the electrical leads brought out from the box.



OUTLINE
ARPA EXP.
RADIO
4-16-74


μPr. + Mem
Power +12
+5
-2
Gr
CLOCK (600MA)
16 ADDRESS/DATA {shared}
Prog I/O, Mem. to dist. device address or Mem Add.
Priority Interrupt (daisy)
DMA priority like above
Int Request
DMA Req.
ACKNOW (DMA or INT)
Read/write
Syst Reset
Addr. Strobe
Data Strobe
Chip Enable

c. Design and Performance Analysis. Multiple detectors work on the virtue that for spread spectrum data communication, with multiple common channels, time discrimination can occur between correlation peaks. With window detectors for data of $3T_c$ chips wide, a blanking signal of $9T_c$ chips wide is used. These particular widths are used primarily because of ease of generation in bit sync for the particular divide ratios used (depending on code length). For timing errors, $9T_c$ blanking signals give overlap so that adjacent correlations will not interfere.

For 420 kBps, the number of chips is 30; thus, three $9T_c$ blanking intervals will be the maximum detectors that could be used.

At 100 kBps, the length is 126. Fourteen blanking signals could conceivably fit in, but would be highly unlikely since no space at all would be between blanking signals. From a composite signal level of processing gain, eight detectors could be allowed if all were at the same signal level. From a practical view, no more than four total detectors is feasible.

One area of concern is establishing Σ and Δ signal levels to a reasonable value. The approach chosen is to power split the multiple detectors output in the signal processing to a common level; e.g., 0 dB gain through the detectors for cascading detectors. Errors in this level would have to be included in the agc range requirements.

Another method of cascading Σ and Δ outputs is to take the Σ and Δ baseband signal and expand. Following detectors would operate coherent agc at baseband rather than at if. This would eliminate some rf amplifiers.

Of course, for multiple detectors to operate satisfactorily, some assumptions and ground rules must be established. These are:

1. Packets may overlap, but preamble must <u>not</u>.
2. Blanking intervals (correlation pulse plus guard band) must not overlap.
3. Composite receive signal levels of multiple packets to single packet signal level must be within 10 dB of each other.
4. ≤ 3 detectors at 420 kBps.
5. ≤ 4 detectors at 100 kBps.
6. ≤ 4 detectors, either at 100 or 420 kBps.

d. Packaging Data. Same as primary signal processing.

e. Control and Monitor. Same as primary signal processing.

f. Power Estimate. Same as primary signal processing.

g. Additional Features. Multiple detectors could be used in repeater and station configurations if network model analysis indicates adequate improved network throughput performance.

8.4 DIGITAL PLAN

8.4.1 General Description

The digital section performs the function of storage and data processing for the packets. It consists of a microprocessor, memory, and control and interface circuits. The functions performed include address recognition, error checking, transmit and receive queuing, header modifications and other network operations defined by the system operating program.

An expanded functional diagram of the digital section is shown in figure 8.4-1. The various functions shown in this diagram are defined in more detail in paragraph 8.4.2.

8.4.1.1 Operational Description

The digital section accepts packet data in serial NRZ format from the signal processing circuits. All the control signals such as SYNC, CLOCK, etc., are provided in the interface. The microprocessor cannot process (check addresses, check packet types, update the header, etc.) the packet data as it is received because the machine cycle time is too slow for the data rates used. Therefore, the packet data goes directly to the random access memory via Direct Memory Access (DMA). The type of DMA used is a "Cycle Stealing" approach. This gives the processor priority on access to memory and allows the data to be processed at a slower rate as it is being received.

If the program can detect any criteria for not receiving a packet, such as a wrong address, the packet is abandoned. The packet may be abandoned before it has been completely received. This allows the system to immediately reinitialize to receive another packet.

As a packet is coming in, a hardware error check is performed to detect any transmission errors. Before any packet is considered good, this error is sampled. If an error has occurred, the packet is abandoned. This decision cannot be made until the entire packet has been received. If the packet is error free, it is accepted for retransmission.

When ready to transmit, the microprocessor raises the TRANSMIT RDY flag to alert the signal processing circuits to switch to the transmit mode. When ready for data, the interface signal TX END-OF-PREAMBLE goes high. The data is then transferred across the interface directly from memory in continuous serial NRZ format. A 16-bit error character is appended to the end of the packet data by hardware error check character generating circuits.

The packet will remain in memory until an acknowledgment is received. Network criteria for repeating and/or rerouting the packet will be determined by the repeater operating program.

The first unit will be implemented with a single detector capable of two data rates. The design is partitioned so that multiple detectors can be used by adding hardware. Up to four detectors can share the memory with the processor and allow input

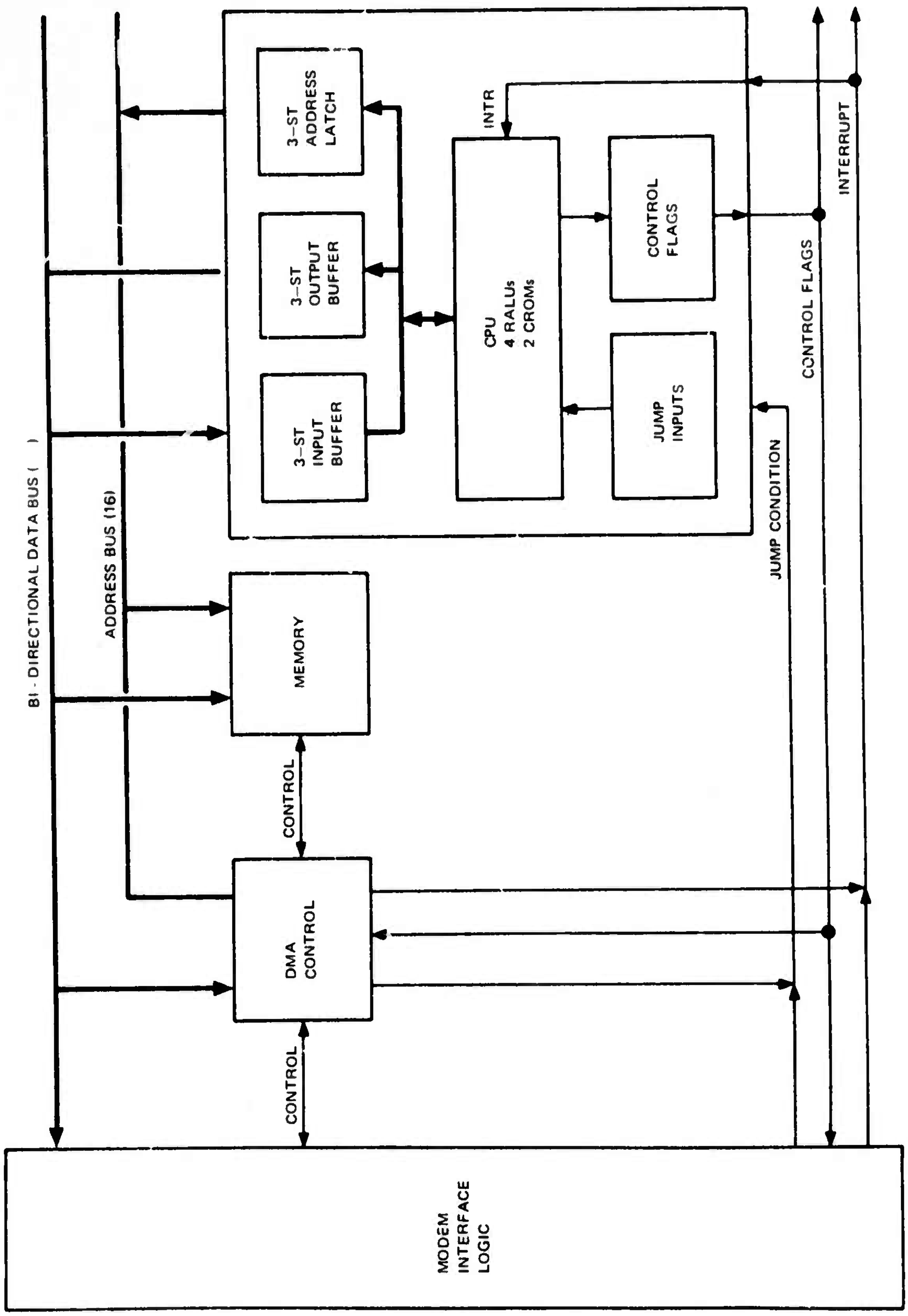


Figure 8.4-1. Digital Section of Repeater, Functional Diagram.

processing to continue. However, the input processing can occur on the input signal from only one detector. The data from other detectors (received concurrently) will simply go to memory for later processing. The queuing logic for handling multiple packets will be a part of the repeater operating program.

The actual transfer of data to and from memory will operate asynchronously with the processor. Prior to receiving or transmitting, the processor will load the DMA counters with the memory starting address and raise a flag to allow the hardware to complete the transfer and inform the processor when complete. The data transfer in the interface and DMA logic is independent of packet format with one exception. When receiving a text packet, the message length is loaded into the receive down-counter (Rx Down Ctr) as the word is received. This allows the packet input to continue and complete without attention from the processor.

The CPU is configured around the National Semiconductor General Purpose Controller/Processor MOS/LSI devices, consisting of two CROM's (Control Read Only Memory) and four RALU's (Register and Arithmetic Logic Units). Each RALU handles 4 bits, and a 16-bit unit is formed by connecting four RALU's in parallel. The organization of the CPU is a modified version of National's IMP-16. The modifications are primarily to reduce power consumption by the use of C-MOS and low power Schottky control circuits, and the addition of features such as the DMA circuits.

Terminal Operation. The microprocessor can be used in the terminal application for the front-end packet handler. Additional terminal operating software and terminal device interface hardware will be required. Low speed terminal devices, such as tty, operator consoles, etc., will transfer data through the processor on an interrupt basis. Thus, software controlled editing and packet formatting can be implemented. The data rates that can be handled using this technique are highly dependent upon the operating software, and a maximum data transfer rate has little meaning without defining the software routine. However, using a handshake word parallel interface, typical data rates of up to 5 kBps should be acceptable.

If high speed terminal devices are used, for example a minicomputer, a block transfer DMA technique as discussed under Station Operation can be implemented.

Station Operation. If the microprocessor is used in the station application as a front-end packet handler, a BLOCK TRANSFER DMA Controller will be required. This function will HALT the microprocessor and transfer packets to/from memory. Using a handshake interface and a 2-μs memory cycle, a maximum transfer rate of 500K words per second can be achieved.

Packet throughput to/from the network will be at the normal repeater rate. Therefore, storage and queuing of packets will perhaps require additional memory.

The station operating program will be different from the repeater program. Also, the block transfer DMA Controller and interface logic are not a part of the repeater and will have to be developed. Many of the circuits required are similar to the packet DMA used in the repeater. However, the requirements are not alike enough to be interchangeable.

8.4.1.2 Design Specification Summary

CPU	National Semiconductor GPCP MOS/LSI Devices
Word Length	16 Bits
Microcycle Time	4 to 8μs — Will be determined by speed/ power tradeoffs in the control circuits.
Memory	2K Words provided 4K Words address structure
Program Storage	Programmable Read Only Memory
Data Storage	C-MOS Random Access Memory
Cycle Time	1.25 Microseconds maximum
Data Transfer	100 kBps to 500 kBps maximum DMA Dual rate implemented
Error Control	16-Bit polynomial generator/check
Number of Detectors	1 Implemented, expand to 4 maximum at 500 kBps maximum
<u>Terminal Application</u>	Requires additional terminal operating software and interface hardware
Data Input	By processor interrupt
Data Output	Word parallel — At terminal device rate with handshake interface
Transfer Rate	Up to 5 kBps (see text)
<u>Station Application</u>	Used as front-end packet handler processor. Requires additional software and block transfer DMA control and interface logic.
Data Input	Block DMA transfer HALT processor
Data Output	Block DMA transfer HALT processor
Transfer Rate	500K words per second maximum Using processor clock

8.4.2 Modem Interface Logic

The modem interface logic provides the interface between the modem and the microprocessor. It will contain the following functions:

Rx Data Serial/Parallel Conversion

Cyclic Redundancy Error Check for Rx Data

Cyclic Redundancy Error Character Generator for Tx Data

Tx Data Serial/Parallel Conversion

Interface Control Signals

8.4.2.1 Primary Interfaces — Modem Interface Logic

Figure 8.4-2 shows the signals in the modem interface and the microprocessor interface. A description of the microprocessor interface signals is given in table 8.4-1.

The modem interface signals are described in paragraph 8.2.1.2.

8.4.2.2 Operating Description

An operating description of the modem interface logic in the repeater environment is given below. The CPU external interfaces are shown in figure 8.4-3.

<u>Receive</u>

Before receiving a packet, the processor will set the FREQ. CONTROL and clear the error circuits. Additionally, the processor will complete its internal initializing and set a starting memory address in the DMA counter. The processor will then set Rx Enable which allows receiving a packet. There is no time limit between Rx Enable and Sync.

When a packet is received, the sync line goes high and the NRZ serial Rx Data is clocked into the serial in/parallel out shift register by the Rx CLK. The data is clocked into the error checking circuits as it is received. A word counter counts 16 bits and raises Rx WORD Rdy to tell the DMA channel that a word is ready to go to memory. The DMA channel has 32 μs at 500 kBps to write the word before it is replaced with the next word in the input data latch. The signal WRITE Rx Wd resets Rx WD Rdy after the word has been written to memory.

The packet data is written to memory on a word basis asynchronously and essentially independent of the processor. The processor is free to begin processing the packet data to determine if it should be receiving this packet, etc. If the packet is not addressed to this repeater, the processor will raise PKT COMPLETE which will reset Rx ENABLE. This will cause the modem to drop sync on this packet. The processor can then reinitialize, set Rx En, and allow receiving a new packet.

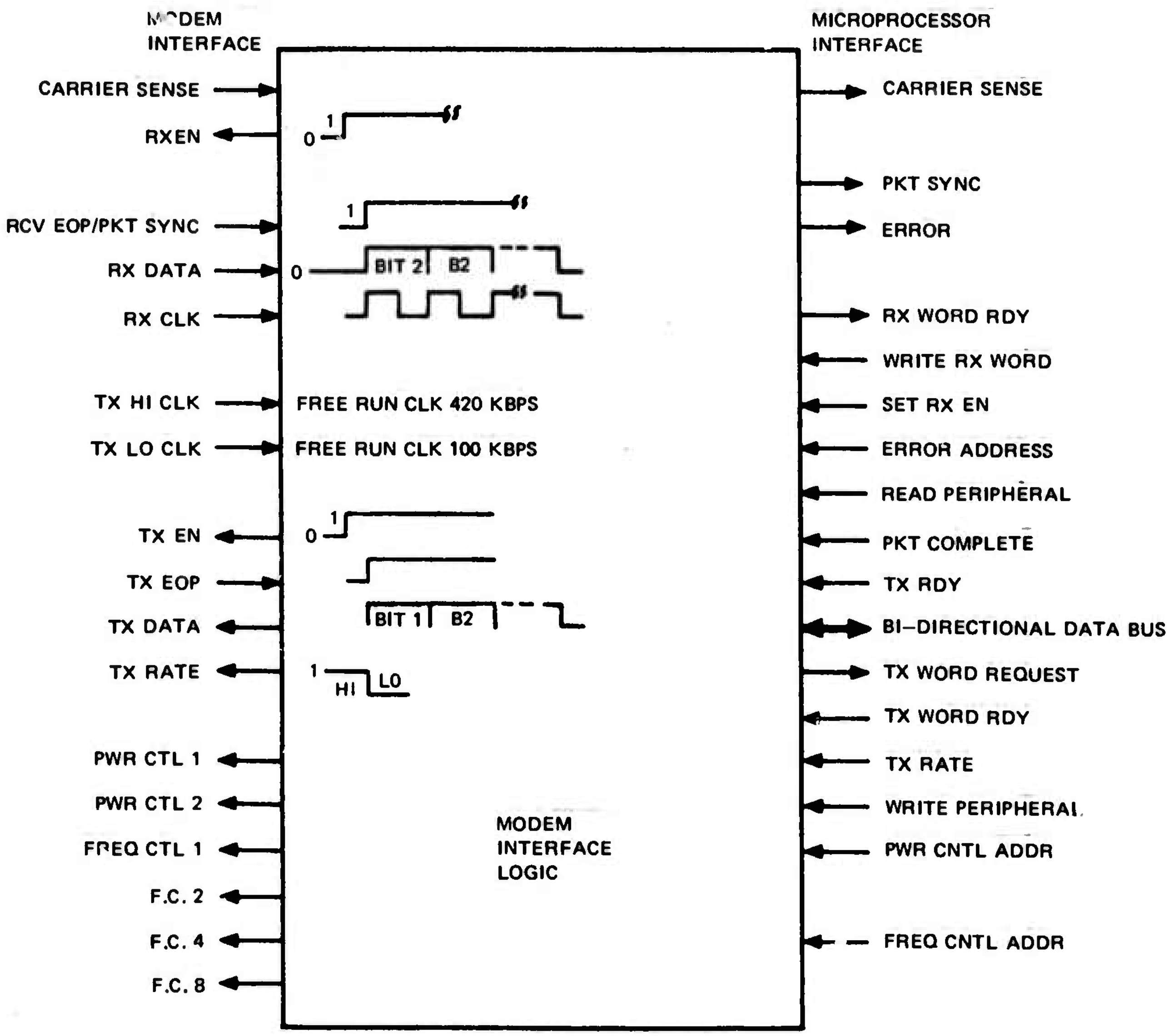


Figure 8.4-2. Signals in Modem Interface and Microprocessor Interface.

Table 8.4-1. Microprocessor Interface Identification.

All mnemonics are shown as true equal +5 volts. Signal absence equals 0 volt. C-MOS circuits are assumed unless otherwise specified. Refer to figure 8.2-1.	
1. Carrier Sense	Same as defined in Modem Interface. Detects presence of rf signal. Optional use by program definition.
2. Packet Sync	Same as defined in Modem Interface. Delimits the start of the received packet.
3. Error	Result of the error check on the Rx packet data. Sampled at end of packet.
4. Rx Word Rdy	Signal that tells the interface that a word is ready to be written to memory. Data must be taken within 32 microseconds after this signal goes high (at 500 kBps Rx rate).
5. Write Rx Word	Enables the tri-state data latch to put the Rx word on the data bus. Trailing edge indicates this word has been written to memory. Trailing edge resets Rx Wd Rdy.
6. Set Rx Enable	After all processor initialization for receiving a packet has been completed, this signal sets Rx En and clears the error circuits.
7. Error Address	A decoded address from the address decode that allows the control flag READ PERIPHERAL to sample the ERROR as a bit on the data bus.
8. Read Peripheral	A processor control flag that allows reading data into the processor on the data bus. Must be used along with the address of a specific data location.
9. Pkt Complete	A signal from the packet DMA controller to indicate the entire packet has been received. The same signal can come from the processor to cause the packet to be abandoned.

Table 8.4-1. Microprocessor Interface Identification (Cont).

10. Tx Ready	After all initialization for transmitting a packet has been completed, this signal sets Tx Enable.
11. Bi-Directional Data Bus	The 16-bit data bus that brings data from the processor or memory and takes data to the processor memory. Data is transferred from/to the data bus with the appropriate control flags.
12. Tx Word Request	Initiates a memory read cycle via the packet CMA controller. A data word must be supplied within 32 μs (at 500-kBps data rate) after this signal goes high.
13. Tx Word Ready	Indicates a data word is on the data bus. Loads the word into the Tx data latch. Resets Tx Wd Req.
14. Tx Rate	Selects the High/Low data rate for transmitting. This signal is selected during the processor initialization for transmitting.
15. Write Peripheral	A processor control flag that indicates data from the processor is on the data bus. Must be used with an address of a specific destination.
16. Power Control Address	A decoded address from the Address Decode that allows the control flag WRITE PERIPHERAL to load the 2 power control bits into the power control latch from the data bus.
17. Frequency Control	Same as above except that this is the specific address that allows loading 4 bits into the frequency control latch from the data bus.

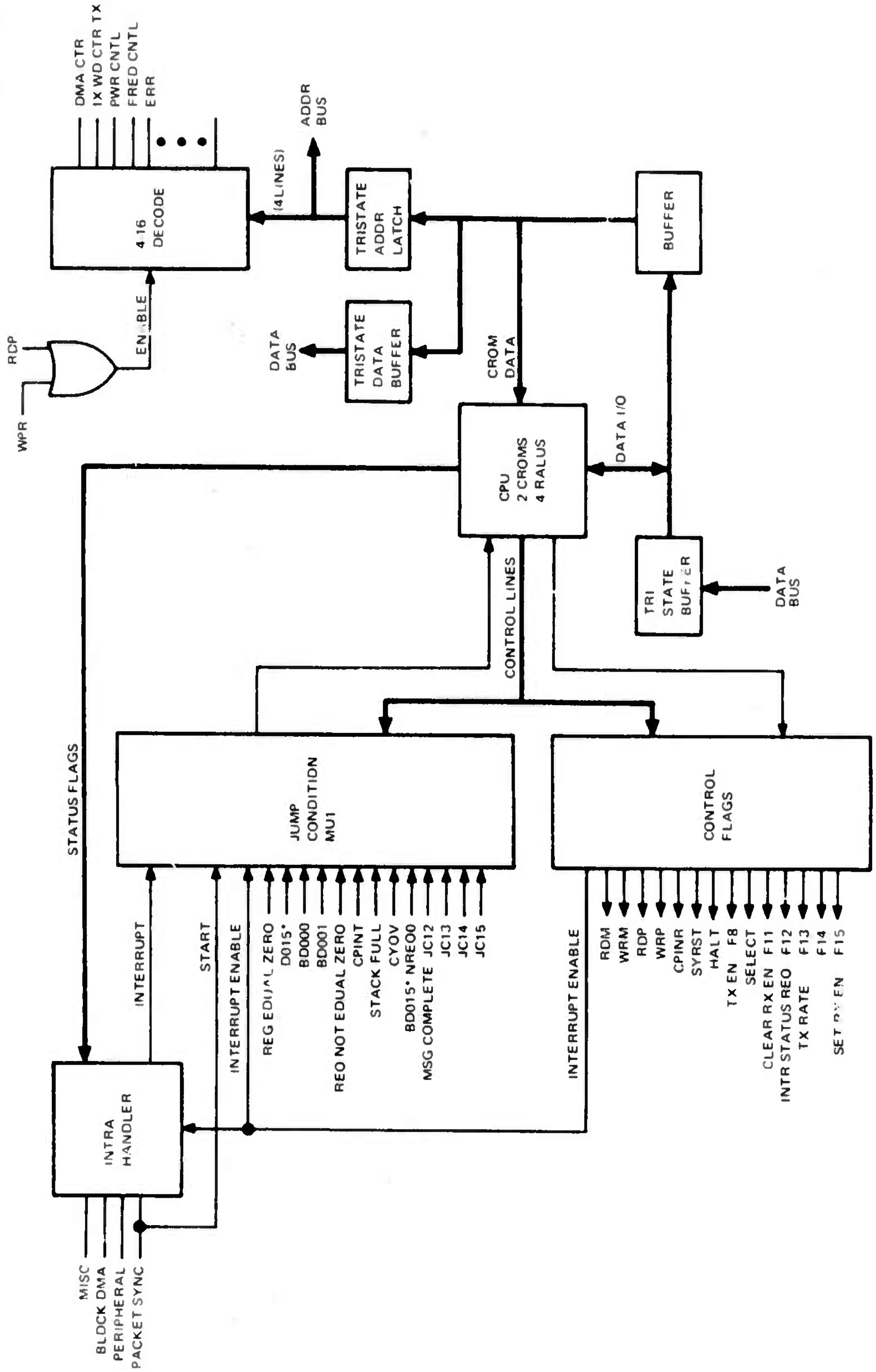


Figure 8.4-3. CPU External Interface.

Transmit

The initialization that must occur before transmitting a packet includes setting the POWER CONTROL bits, selecting the Tx Rate, loading the DMA channel with the memory starting address, and checking CARRIER SENSE. POWER CONTROL is set by decoding a PWR CNTL ADDRESS and outputting data on the Data Bus along with a WRITE PERIPHERAL flag. The Tx Rate is selected in the same manner.

When ready to transmit the processor raises Tx Rdy. Tx Rdy will set Tx Enable in the interface logic and cause the modem to go into the transmit mode. The first word will be fetched from memory by raising the Tx WORD REQUEST line. This word will be received as data on the Tx Data Bus along with the Tx WORD RDY flag. The word will be loaded into the parallel input/serial output shift register.

After the preamble has been sent by the modem, the Tx End-of-Preamble flag will go high and cause the Tx Data to be shifted to the modem. The Tx EOP will also cause a Tx Wd Req. to fetch the next word. A word counter will count the bits as they are shifted out and initiate a Tx Wd Req every 16 bits. As the Tx data is shifted out, the error character generator will accumulate an error character to append to the end of the packet.

The DMA controller will signal when the last Tx word has been ready from memory. The error character will then be added to the data and when the last bit has been shifted across the interface, TX EN will be reset.

8.4.2.3 Repeater, Terminal and Station Applications

The modem interface logic can be identical for all applications. For the terminal and station, this logic along with the microprocessor can perform the packet handling functions as it does in the repeater. Different operating programs and disciplines will be followed for the appropriate I/O interfaces, but the packet in/packet out operating procedures and hardware can remain the same.

8.4.2.4 Physical and Electrical Characteristics

Three circuit boards of 5-inch by 5-inch size will be required for packaging. The functions of packet Rx and packet Tx will be partitioned as separate circuit boards. This will allow adding increments of packet Rx logic for multiple detectors.

The voltage required will be +5 volts and the estimated power is less than 500 milliwatts.

8.4.3 CPU

The CPU is configured around the National Semiconductor GPC/P MOS/LSI devices, as shown in the simplified block diagram of figure 8.4-4. The MOS/LSI devices consist of two CROMS and four RALU's. Each RALU handles 4 bits, and a 16-bit unit is formed by connected four RALU's in parallel. A 4-bit-wide control bus is used by the CROM to communicate most of the control information to the RALU's.

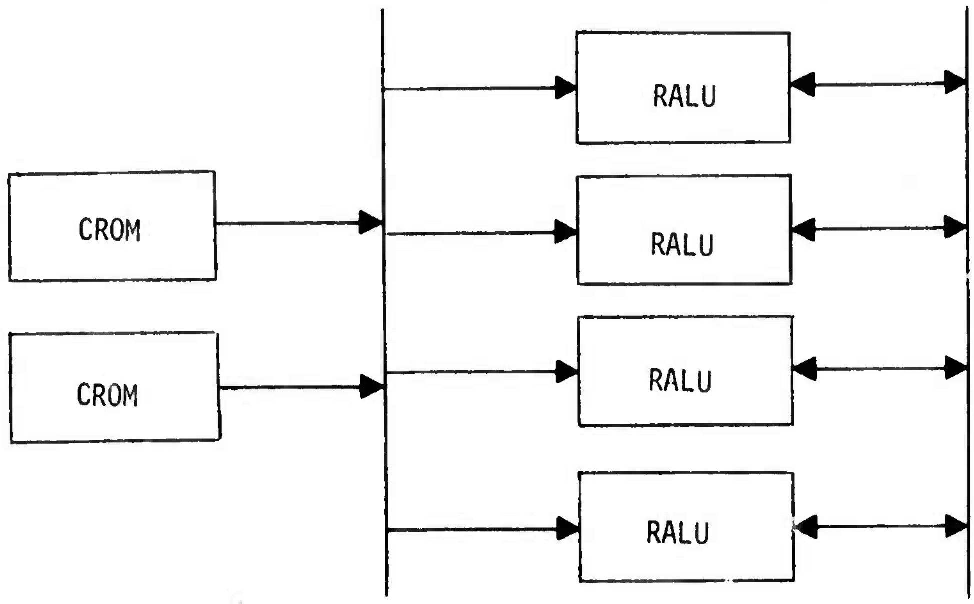


Figure 8.4-4. IMP-16 CPU Components.

The CROM's control the operation of the CPU. The control is effected by routines that constitute the microprogram stored in the read only memory of the CROM's. The microprogram effects the implementation of macroinstructions that comprise the IMP-16 Instruction Set.

There are three circuits which allow the IMP-16 to interface to external circuits that wish to communicate with the IMP-16. Conditional branches are selected by the conditional jump multiplexer. Control flags are manipulated by the CPU to define and control operations. The two previous circuits are external to the CPU devices. Internal to the devices are the status flags, some of which can be seen externally.

There are 16 control flags that can be set or pulsed by the CPU. Eight of these are processor controlled and are not usable by the programmer, but can be used for defining the operations being performed by the CPU. Eight control flags may be accessed by macroinstructions. Two of these are defined for specific uses, interrupt enable and select carry/overflow, and six are user specified. Table 8.4-2 indicates the assignment of these control flags.

A 16 to 1 multiplexer is used to gate 16 jump conditions into the one conditional branch input of the CPU. The CPU sends a 4-bit number to define which condition is sampled. Twelve of the inputs are defined by the CPU microprogramming and four are user defined. Any of the 16 can be addressed by a branch-on-condition instruction. Three of the 12 assigned can be used by the user. They are interrupt, control panel interrupt, and start. Table 8.4-3 indicates the assignment of the four user defined jump condition inputs.

Table 8.4-2. Control Flag Assignments.

F8	Transmit Ready
F11	Packet Abandon
F12	Set Receive Enable
F13	Interrupt Status Request
F14	Transmit Rate
F15	Not Used

Table 8.4-3. Jump Condition Assignments.

JC12	Message Complete
JC13	Tx Complete
JC14	Not Used
JC15	Not Used

There are 16 RALU status flags. Whenever the status flags are manipulated, the entire complement of flags is configured as a 16-bit register. The L (link), CY (carry), and OV (overflow) flags are the first, second, and third most significant bits, respectively, and the remaining general-purpose flags comprise 13 less-significant bits. Bits 0, 4, 8, and 12 are used as IEN0, IEN2 and IEN3, respectively, which are the interrupt enable flags for each of the four levels defined in the interrupt handler, figure 8.4-5.

CPU-Packet Interface

The previous section covered the circuits available for interfacing to the CPU. This section will define how the packet control signals enter the processor to tell it a packet has arrived. The processor has no real-time knowledge of a packet being stored in memory since this is done asynchronous to the processor. When the processor is told a packet is ready for processing, the extent of its knowledge about the packet is where it is located in memory. The prerequisite to any communications with the CPU is to get its attention. The primary means of doing so is through the interrupt handler.

The repeater will have a multilevel interrupt handler. As shown in figure 8.4-5, there are four processor interrupt request levels plus a stack overflow interrupt request. All peripheral devices for one level are wired to the single input line for that level. The processor responds to inputs on the interrupt request lines which are labeled IRREQ0 through IRREQ3. There is a separate interrupt enable flag for each of the four interrupt levels (labeled IEN0 through IEN3) and a master interrupt enable (labeled INTEN) for all four levels plus the stack overflow interrupt. The interrupt enable flags for each individual level are part of the CPU status flags. The INTEN flag is one of the CPU control flags.

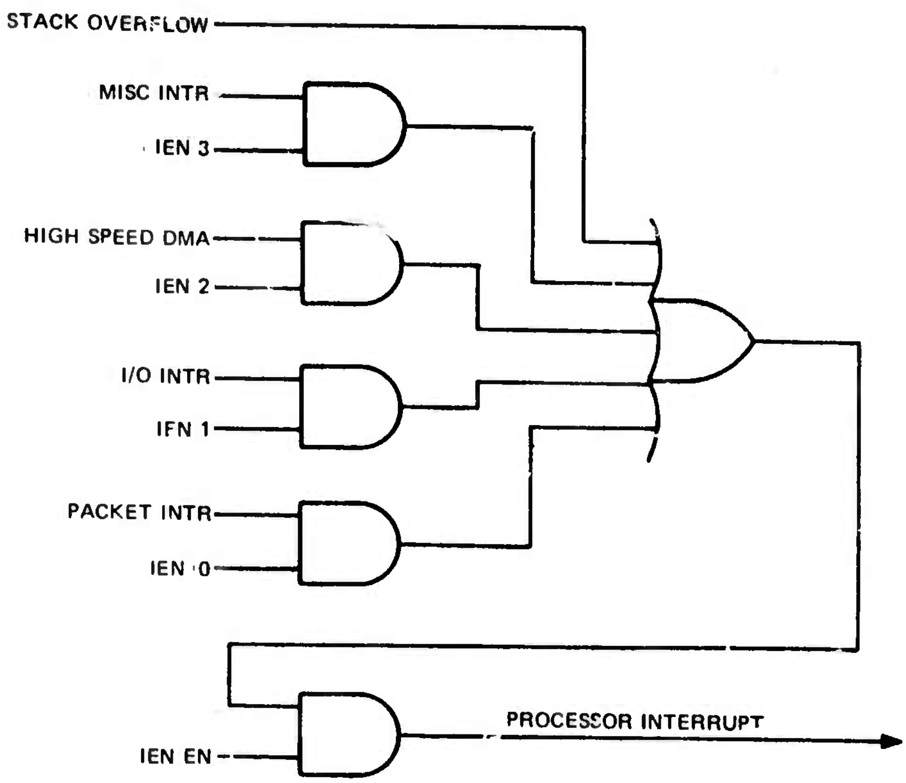


Figure 8.4-5. Interrupt Handler Circuit.

The interrupt request levels will be defined as follows:

Level 0 - Packet Sync Interrupt Request

Level 1 - Peripheral Interrupt Request

Level 2 - High Speed DMA Interrupt Request

Level 3 - User Defined

The interrupt handler allows maximum flexibility of the repeater. By changing software and adding some hardware, the repeater can be used in a terminal or station application.

Single Detector Packet-CPU Interface

Packet sync enters the processor through the interrupt handler circuit and the start jump condition multiplexer (JCM) input. A message complete signal enters through another jump condition multiplexer input. The processor may be executing or in a halt state when a packet is received.

If a repeater is idle, the processor could be in a halt condition. To restart the processor, the start line must be pulsed. When this is done, the processor clears the halt flag, steps the program counter (PC) and fetches the next instruction. To prevent an interrupt from the packet sync when the first instruction is executed, the interrupt enable for the packet sync level must be disabled.

In the case of program execution, the processor will store the PC and jump to the interrupt service routine to determine what is interrupting. The packet sync could be given highest priority by checking it first. This can be accomplished by looking at the start JCM input rather than going through the interrupt circuit.

One JCM input will be fed by a message complete flip-flop. It will be set at the end of the packet. This tells the processor when to check the error circuit. The MSG complete FF is cleared when the processor reads the error flip-flop. Figures 8.4-6 and 8.4-7 diagram the signals entering the processor.

Optional Multiple Detectors

The handling of multiple detectors is significantly more difficult than a single detector. Determination of which detector is receiving or has received a packet and bookkeeping of packet data cause the software to be more complex and time consuming.

All packet interrupt requests will be tied to a flip-flop and then to the processor interrupt. The processor could disable level 0 interrupt request and clear the packet sync FF. This would allow the processor to know if a packet had entered the repeater while it had been processing the previous packet.

The packet sync from each detector will be tied together to the start JCM input. This will serve two functions. It allows the processor to look at the packet syncs to determine if a packet is currently being received. The repeater cannot transmit while it is receiving. This input also serves to get the processor out of a halt state when a packet is received.

The message complete flip-flops will be tied together to a JCM input.

To determine the status of the individual detectors, the processor must execute a RIN with the proper address for the detector status register. The register will consist of packet sync, MSG complete, and error bit for each detector. This is indicated in figure 8.4-8.

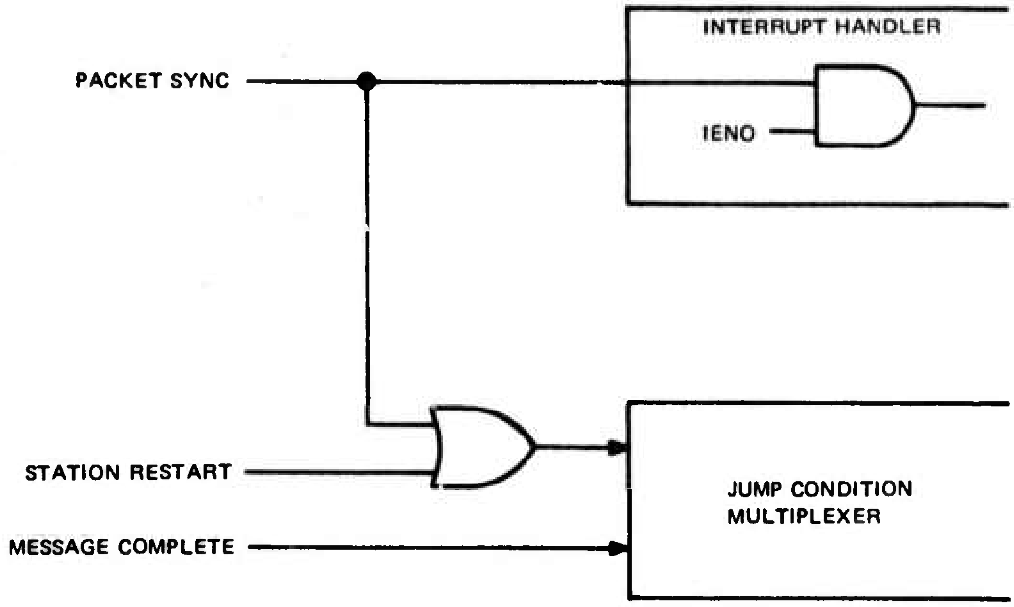


Figure 8.4-6. Single Detector Interrupt.

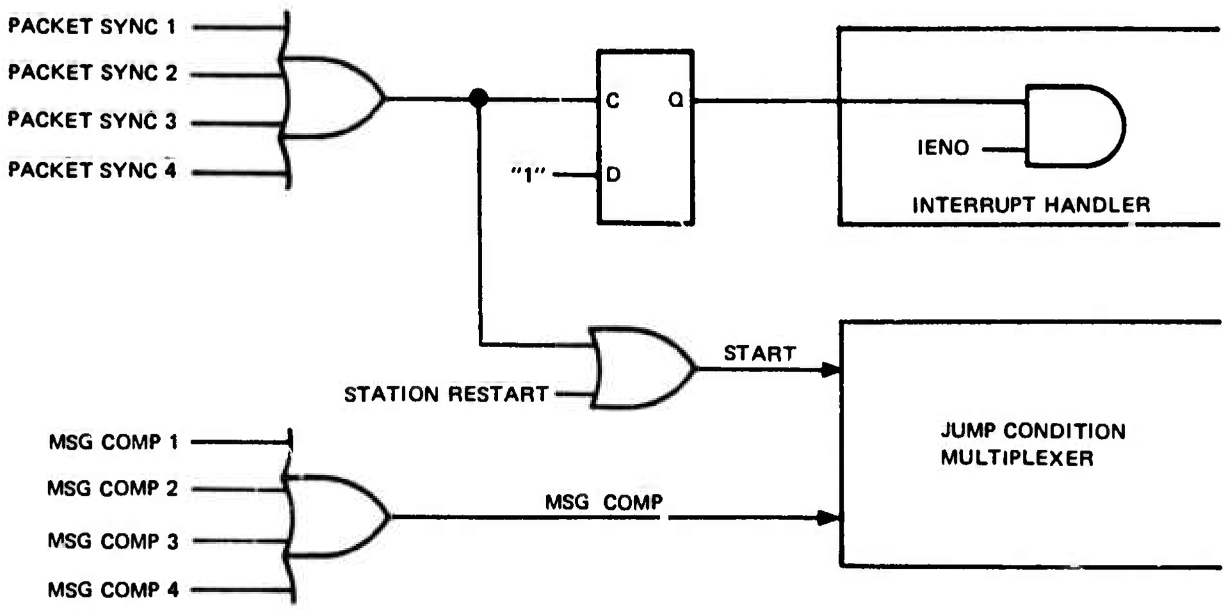


Figure 8.4-7. Multiple Detector Interrupt.

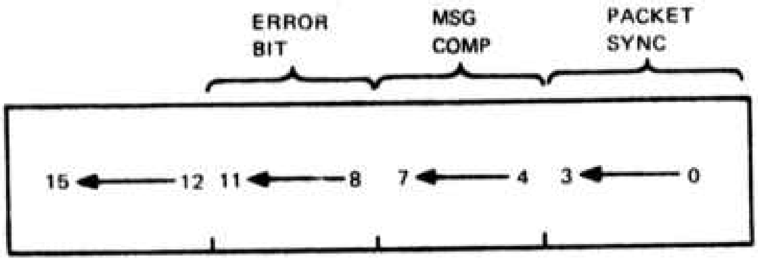


Figure 8.4-8. Detector Status Register.

The packet-processor communications will not be affected in hardware by use as a terminal or station. The software will be the only factor affecting the operation. If the repeater is used in a station application, the start JCM input will be shared by the packet sync and station restart. These two signals should not conflict. The station restart signal is produced during a high speed DMA between repeater memory and station memory. To allow a high speed DMA, the repeater processor must place itself in a halt state while the memory is being accessed and be restarted when the transfer is complete.

Figure 8.4-7 is a diagram of the multiple detector signals.

Address and Data Bus Communications

Another means of CPU communications is through a register out or register in instruction. This is the method used when the CPU needs to transfer data as well as control information such as loading the DMA counter with the beginning address of the packet buffer. This is also the means of communication between peripheral devices.

When a ROUT instruction is executed, data and address are taken from the CPU registers and placed on the data bus and address bus and the write peripheral (WRP) control flag is pulsed. Using the WRP as a gating signal, the address is decoded by a 4- to 16-line decoder. These outputs are then used to gate the data on the data bus into the proper device.

RIN instructions function in the same manner as the ROUT except that data is taken into the CPU when the read peripheral flag is pulsed.

In a single detector repeater, 6 of the 16 decoded address lines are used. Table 8.4-4 indicates the devices being addressed. In a multiple detector repeater, nine address lines are needed. Table 8.4-5 is a list of the devices.

The unused decoded address lines could be used in a terminal or station application where some peripheral devices would need to interface with the CPU.

8.4.4 Memory

The memory will consist of 1024 words (16 bits) of Random Access Memory (RAM) and 1024 words of Programmable Read Only Memory (PROM). The address decode will provide for an additional 1024 words each of RAM and PROM.

Table 8.4-4. Single Detector Repeater.

DEVICE	NUMBER	TYPE OF INSTRUCTION
DMA Counter	1	ROUT
TX Word Counter	1	ROUT
Power Control	1	ROUT
Frequency Control	1	ROUT
Error Bit	1	RIN
Maintenance Console	Up to 11	RIN-ROUT

Table 8.4-5 Multiple Detector Repeater.

DEVICE	NUMBER	TYPE OF INSTRUCTION
DMA Counter	4 Maximum	ROUT
TX Word Counter	1	ROUT
Power Control	1	ROUT
Frequency Control	1	ROUT
Detector Status Register	1	RIN
Maintenance Console	Up to 8	RIN-ROUT

The addressing structure will locate the RAM at the low order address bits and the PROM at the high order bits. This is listed below.

	Memory Implemented	Memory Not Implemented
	0-1023	1024-2047
RAM ADDRESSES	0000-03FF HEX	0400-07FF HEX

	Memory Not Implemented	Memory Implemented
	63,488-64,511	64,512-65,535
PROM ADDRESS	F800-FBFF HEX	FC00-FFFF HEX

Memory is defined and divided in terms of pages. A page is 256 words of storage. The addressing structure and decode is shown in figure 8.4-9. As shown in this figure, pages 5, 6, 7 and 8 of RAM and pages 249, 250, 251 and 252 of PROM can be added by simply providing the memory circuit boards and wiring.

Figure 8.4-10 shows a typical page of RAM and figure 8.4-11 shows four pages of PROM.

RAM. A C-MOS RAM will be used that is 256 x 1 bit. For 256 words, 16 paks will be required. For 1024 words, 64 paks are required.

A single power source of +5 volts is required. The electrical properties are listed below:

	256 x 1	1024 x 16
QUIESCENT DEVICE CURRENT	$5\mu^{\underline{a}}$	$320\mu^{\underline{a}}$
QUIESCENT PKG DISSIPATION	$25\mu^{\underline{w}}$	$1.6M^{\underline{w}}$
READ CYCLE TIME	1.2 μs	
WRITE CYCLE TIME	1.2 μs	

PROM. The programmable read only memory is a p-channel, MOS/LSI device that is organized as a 256 x 8-bit memory. Two devices are required to give 256 words of storage. For 1024 words, eight devices are required.

The power source required is +5 volts and -12 volts. The electrical operating properties are listed below:

	256 x 8	1024 x 16
QUIESCENT DEVICE CURRENT	$55M^{\underline{a}}$	$440M^{\underline{a}}$
ACCESS TIME	1 μs	

PACKAGING. Assuming a circuit board size of 0.5 inch x 0.5 inch one page of RAM (16 paks) or four pages of PROM (8 paks) can be put on each circuit board.

RAM	256 words per board, 1024 words = 4 circuit boards
PROM	1024 words per board = 1 circuit board

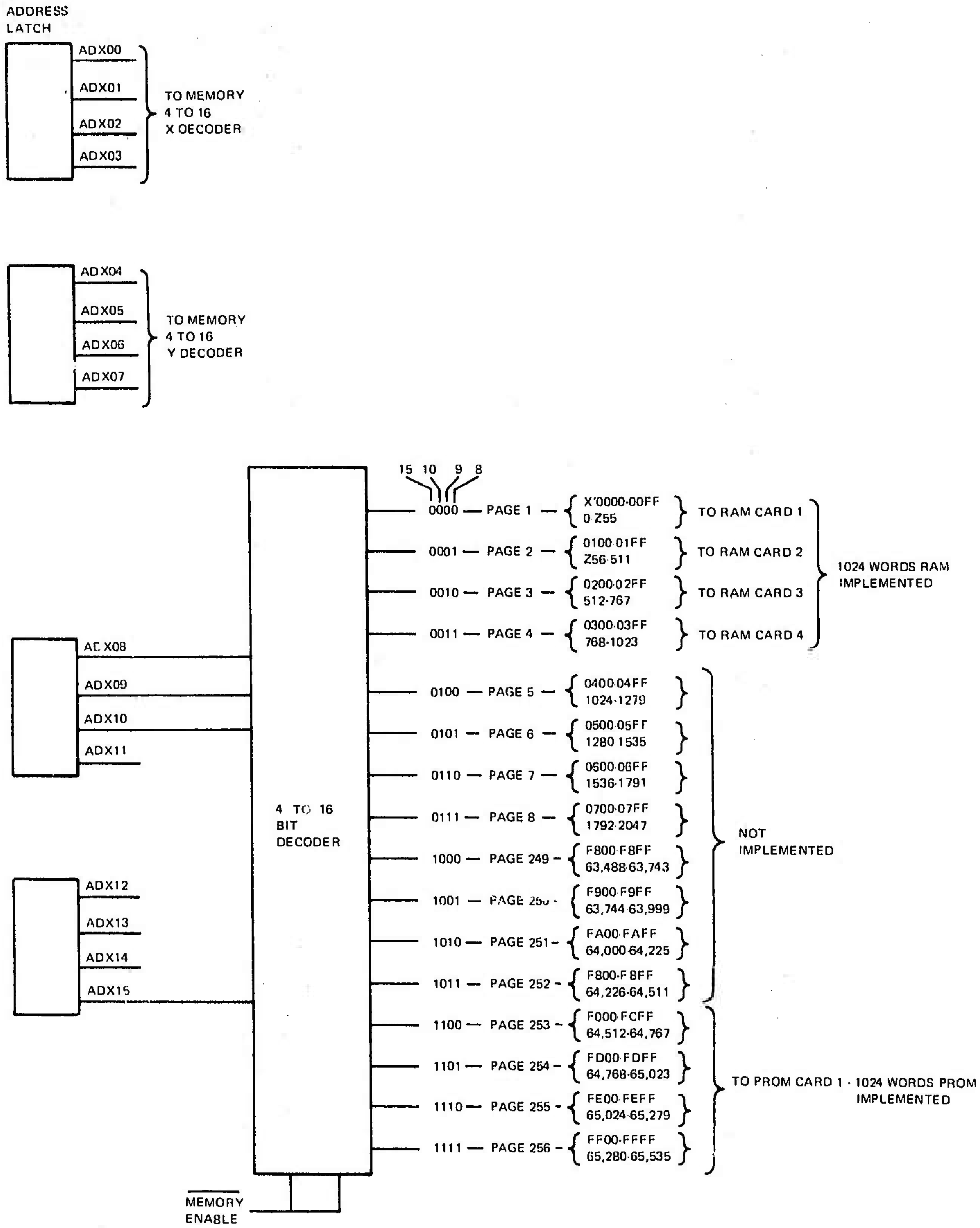


Figure 8.4-9. Memory Address Structure.

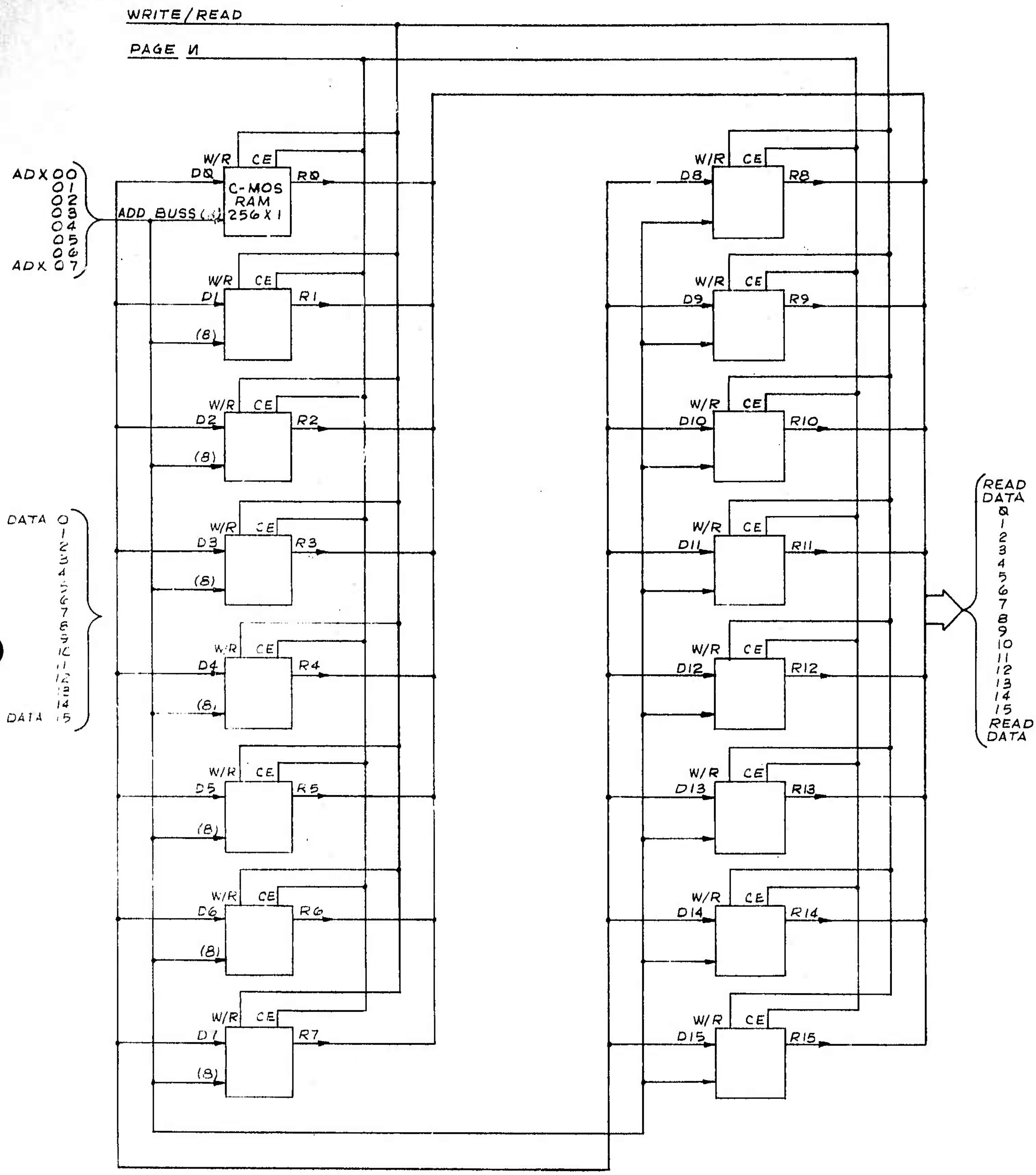


Figure 8.4-10. Typical RAM Structure (256 Words).

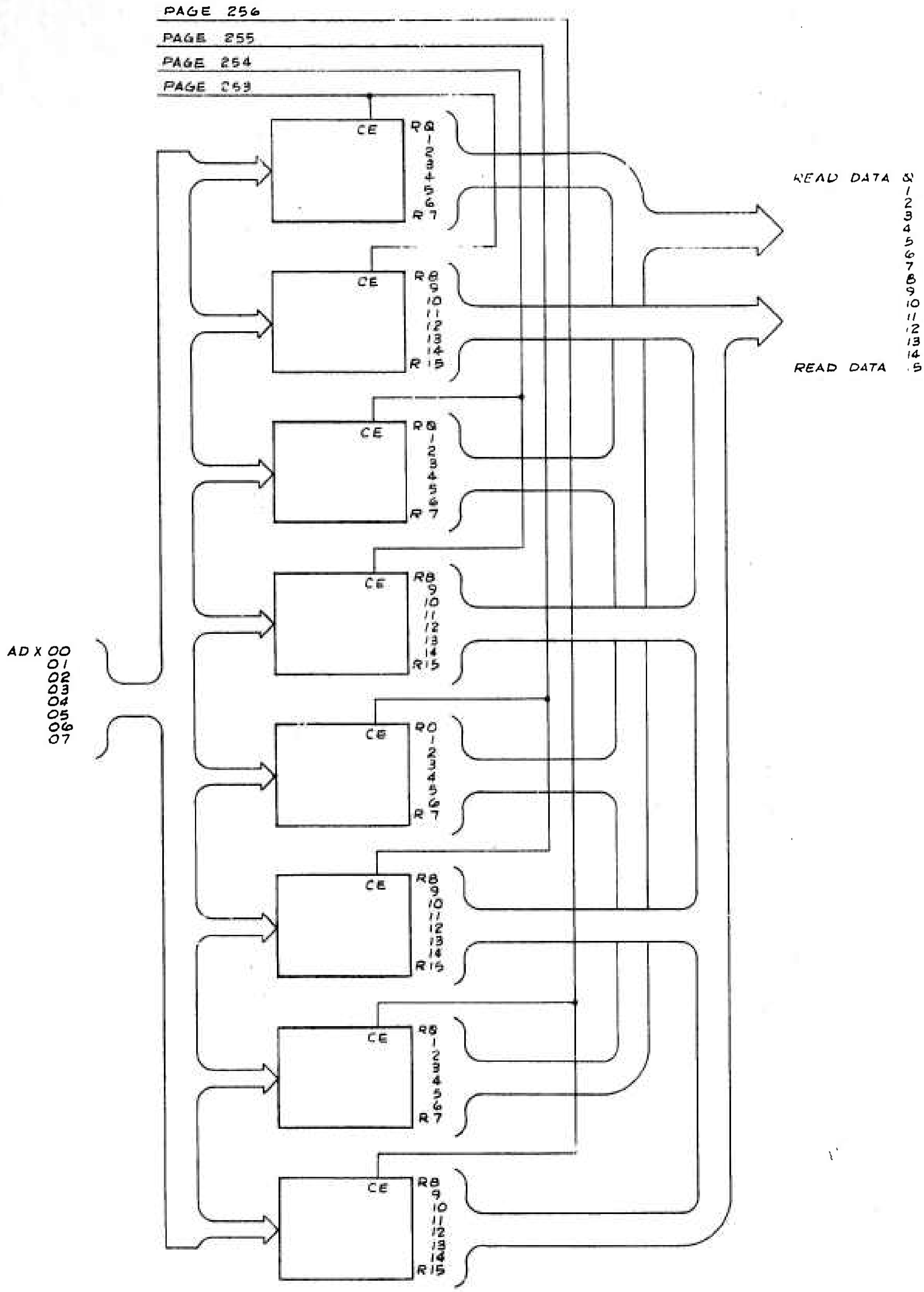


Figure 8.4-11. Typical PROM Structure (1024 Words).

8.4.5 Memory Control

A block diagram showing the elements of memory control is shown in figure 8.4-12. Control of memory is shared by application as listed below:

CPU	Has priority control of memory in the repeater application.
PACKET DMA	Takes control of memory in a "cycle stealing" basis. The packet DMA control can have memory when the CPU is not using it.
BLOCK DMA	Transfers packets to/from memory at high data rates. The processor must HALT for a BLOCK DMA transfer. This transfer is initialized/terminated by using the INTERRUPT/START inputs to the CPU. The application for this is in the station where the repeater hardware is used as a front-end packet handler. Additionally, this function could be used at a terminal where high speed I/O devices (for example, a minicomputer) may be used. The logic (HARDWARE) for this option is NOT included as a part of the repeater logic. However, the design of the repeater has considdred this application so it can be implemented as an appendage.
BUS CONTROLLER	Resolves contention for memory between the CPU and the packet DMA.
READ/WRITE CONTROL	Generates the timing signals for accessing memory.

8.4.5.1 Packet DMA (Figure 8.4-13)

The packet DMA circuit provides the memory addressing during I/O, and determines the End of Packet. Included in this section are the DMA address counter, receive word counter, transmit word counter, and associated control circuitry.

The DMA address counter provides the memory addressing during direct memory access of packet data. It serves this function on transmit and receive. The counter is a 16-stage presettable counter, which allows any location in memory to be addressed. The DMA counter must be loaded by the processor with the starting address of the packet buffer before setting the receiver or transmit enable flip-flops. The counter is loaded by executing a ROUT Instruction with the proper address for the DMA counter. The tri-state output of the DMA counter is connected to the address bus and is enabled whenever packet data is to be transferred. The counter is stepped after each memory access.

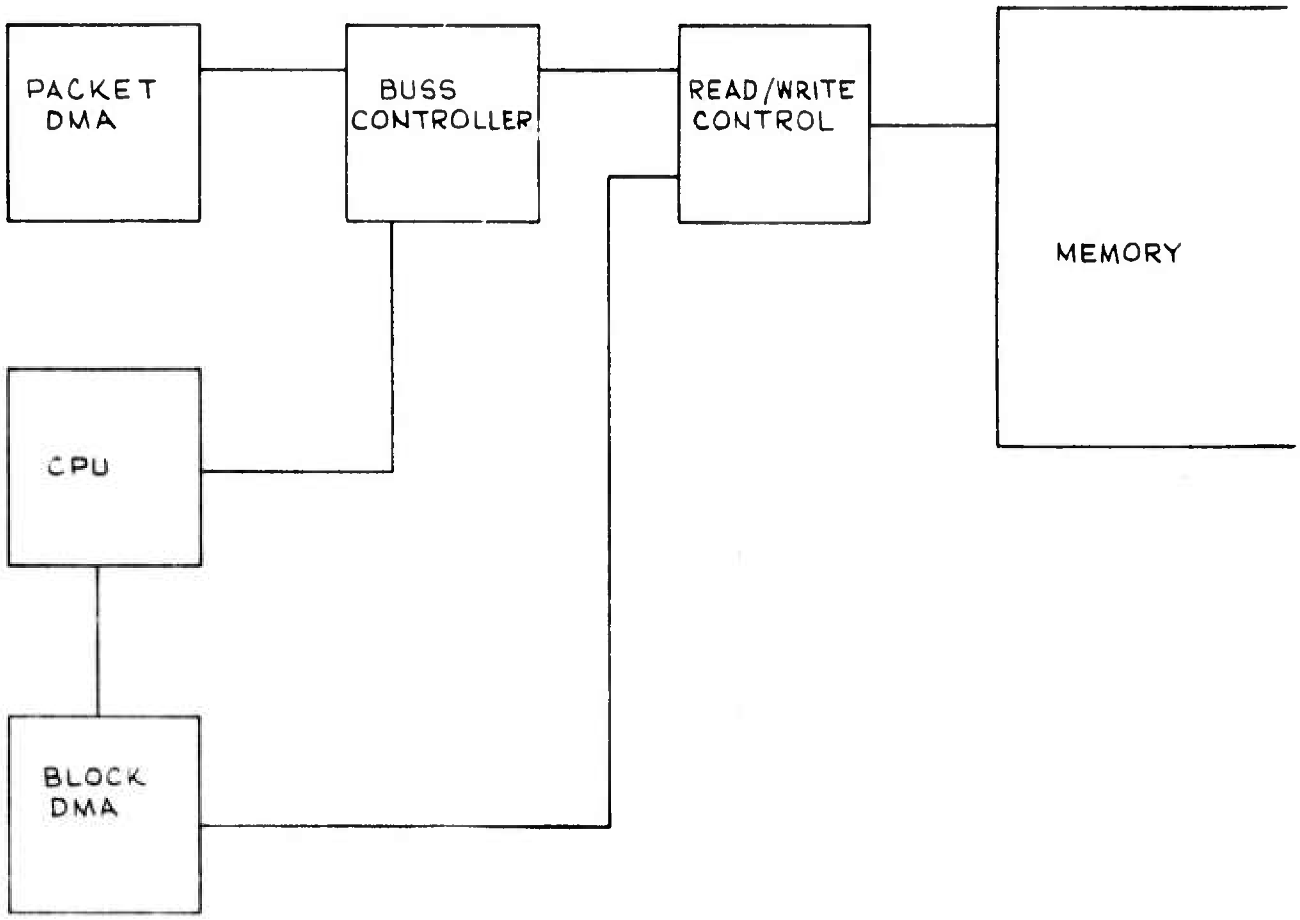


Figure 8.4-12. Element of Memory Control.

The receive word counter (Rx Wd Ctr) provides timing on a word basis to determine key points within a packet and the end of the packet. The 8-stage presettable up/down converter is clocked every 16 bits and is cleared by sync. At the beginning of a packet, the Rx Wd Ctr counts up. During the first word time, the Text/hdr FF is loaded with the Text/Hdr bit. After counting five more words (the remainder of the header), the counter does one of two things depending on the Text/Hdr bit. If the packet was a header only, the counter advances one more count to allow the error word to enter the error check circuit and then clears the receive enable flip-flop. If the packet was a header and text, the counter advances one count and loads a byte (8 bits) of the next word (first word of text) into itself. This byte contains the number

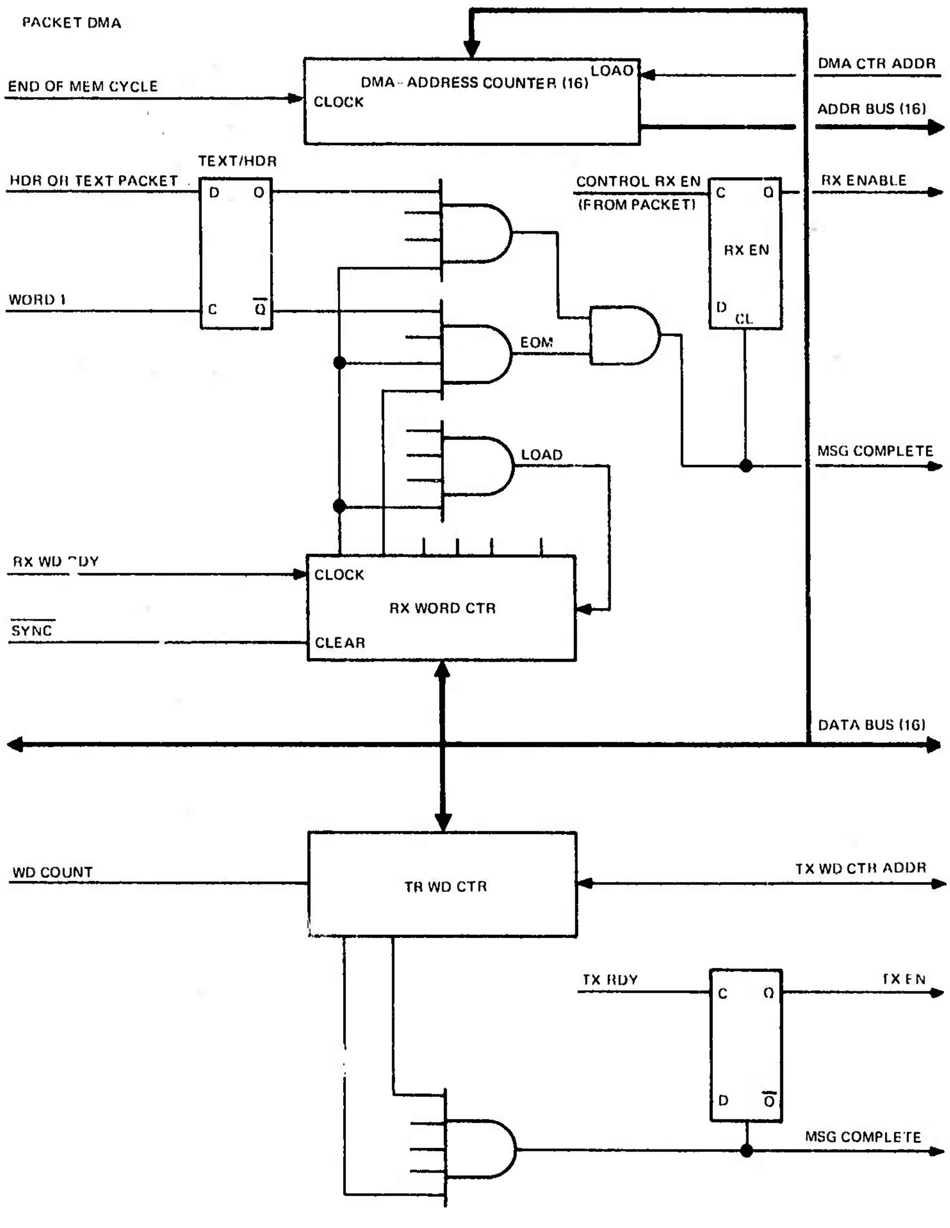


Figure 8.4-13. Packet DMA,

of words in the text. The counter counts down to zero from this point. When zero is decoded, the receive enable flip-flop is cleared.

The transmit word counter (Tx Wd Ctr) serves a function similar to the Rx Wd Ctr. The Tx Wd Ctr is loaded before the Tx En FF is set with the number of words to be transmitted (the sum of the header and text length). The counter is loaded by executing a ROUT Instruction with the proper address for the Tx Wd Ctr. Counting down, the Tx Wd Ctr reaches zero, gates the error word onto the serial data bus, and clears the Tx En FF.

The packet DMA circuit can do the packet handling function as described above for the repeater in both the terminal and station application.

8.4.5.2 Packet DMA Bus Controller

The digital section of the repeater has two bi-directional buses: The Address Bus and the Data Bus. The processor uses the buses whenever needed. The DMA bus controller determines when the processor is not using the buses and allows packet data to be stored or removed from memory directly. The bus controller timing diagram is shown in figure 8.4-14 and the logic diagram in figure 8.4-15.

A microprocessor instruction cycle is a sum of several microcycles. Each microcycle is divided into eight time periods, T1-T8. The bus controller defines two bus cycles during each microcycle. The processor sets control flags at the beginning of T2 which define the bus cycles to be used during that microcycle. If the microprocessor executes a write memory (WRM) or a write peripheral (WRP), it will do so during bus cycle 1. If the microprocessor executes a read memory (RDM) or read peripheral (RDP), it will do so during bus cycle 1. Any bus cycle the microprocessor does not use may be used by the DMA for a read or write memory.

Bus cycle 1 begins halfway through T2 and ends halfway through T4. Period T4 is extended two periods during a memory access to accommodate the memory access times. Bus cycle 2 begins at T5 and ends at the beginning of T8. Cycle 2 is slightly longer than cycle 1 because of the microprocessor requirement that data being read be present for the entire T7 period. In bus cycle 2, T6 is extended two periods to allow for the memory cycles.

The bus controller is designed to accommodate up to four detectors simultaneously. The processor can be processing a packet while receiving four packets. The data rate may be up to 500 kBps maximum on any detector.

To implement one detector requires eight CMOS IC's. Each additional detector will require two IC's.

No design differences exist between repeater, terminal, or station applications for the DMA bus controller. In a terminal application all processor-I/O data must pass through the processor, which means it has control of the bus. In the station application, the processor disables packet communication and gives control of the bus to the high speed data transfer controller.

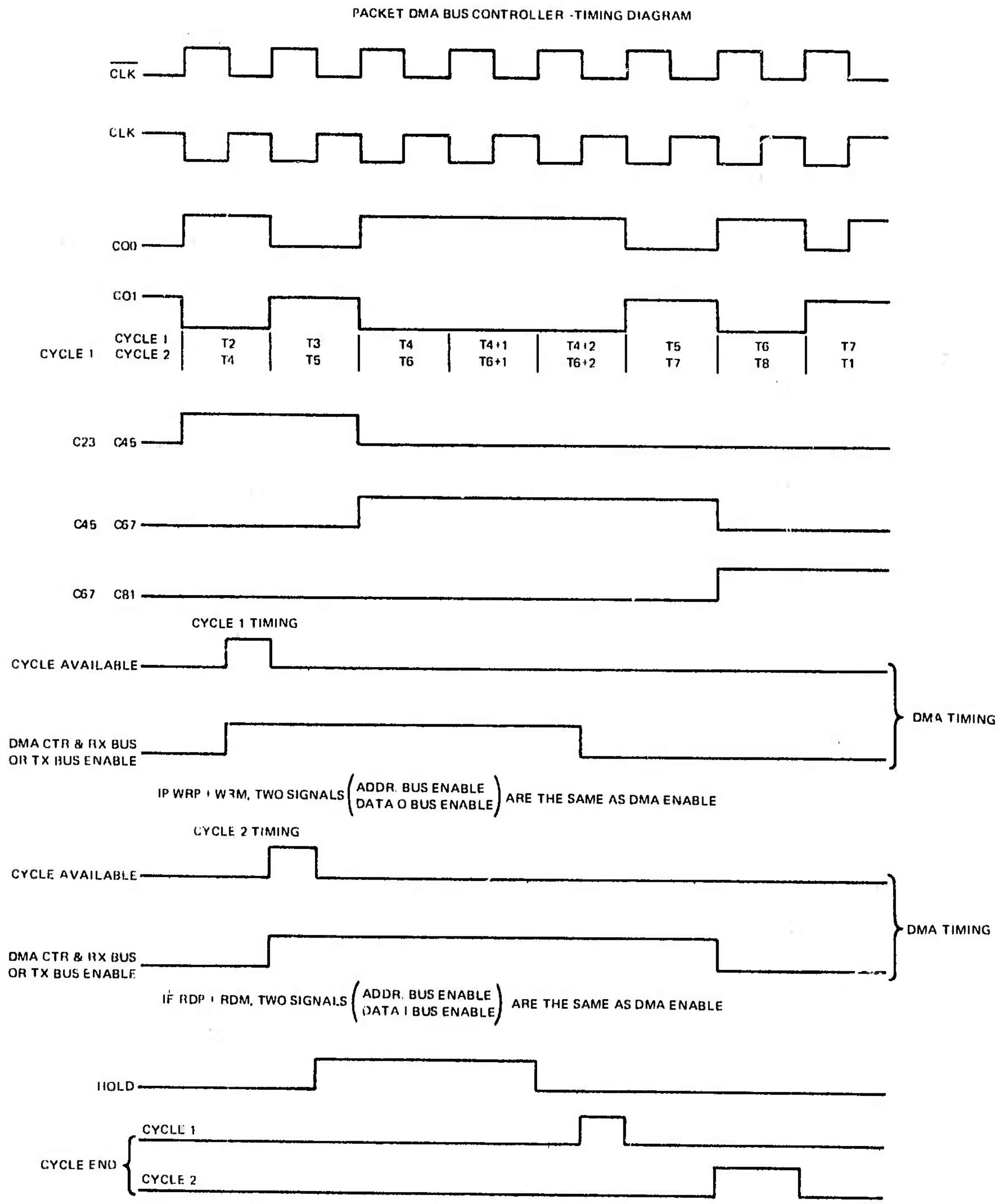


Figure 8.4-14. Packet DMA Bus Controller Timing Diagram.

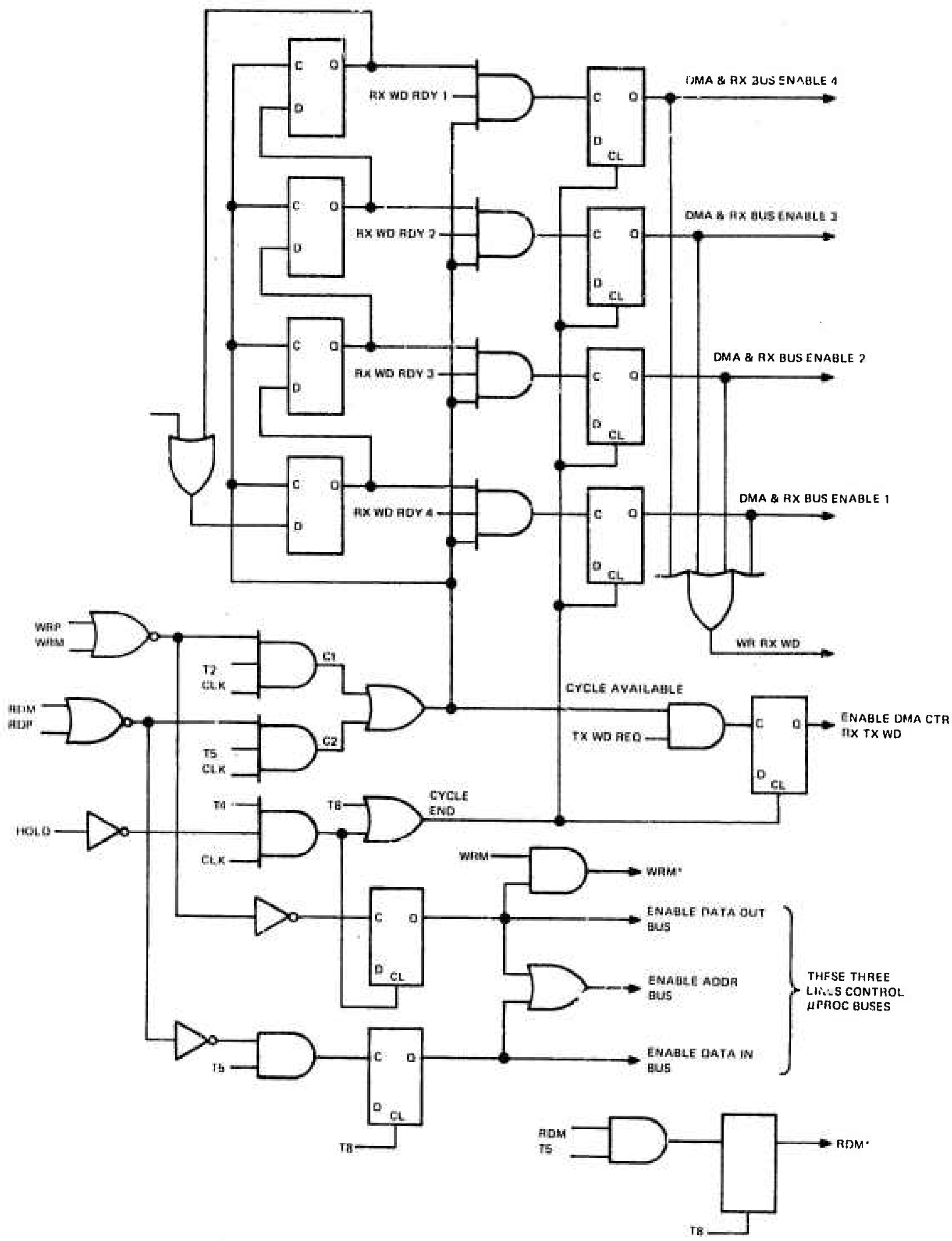


Figure 8.4-15. Bus Controller.

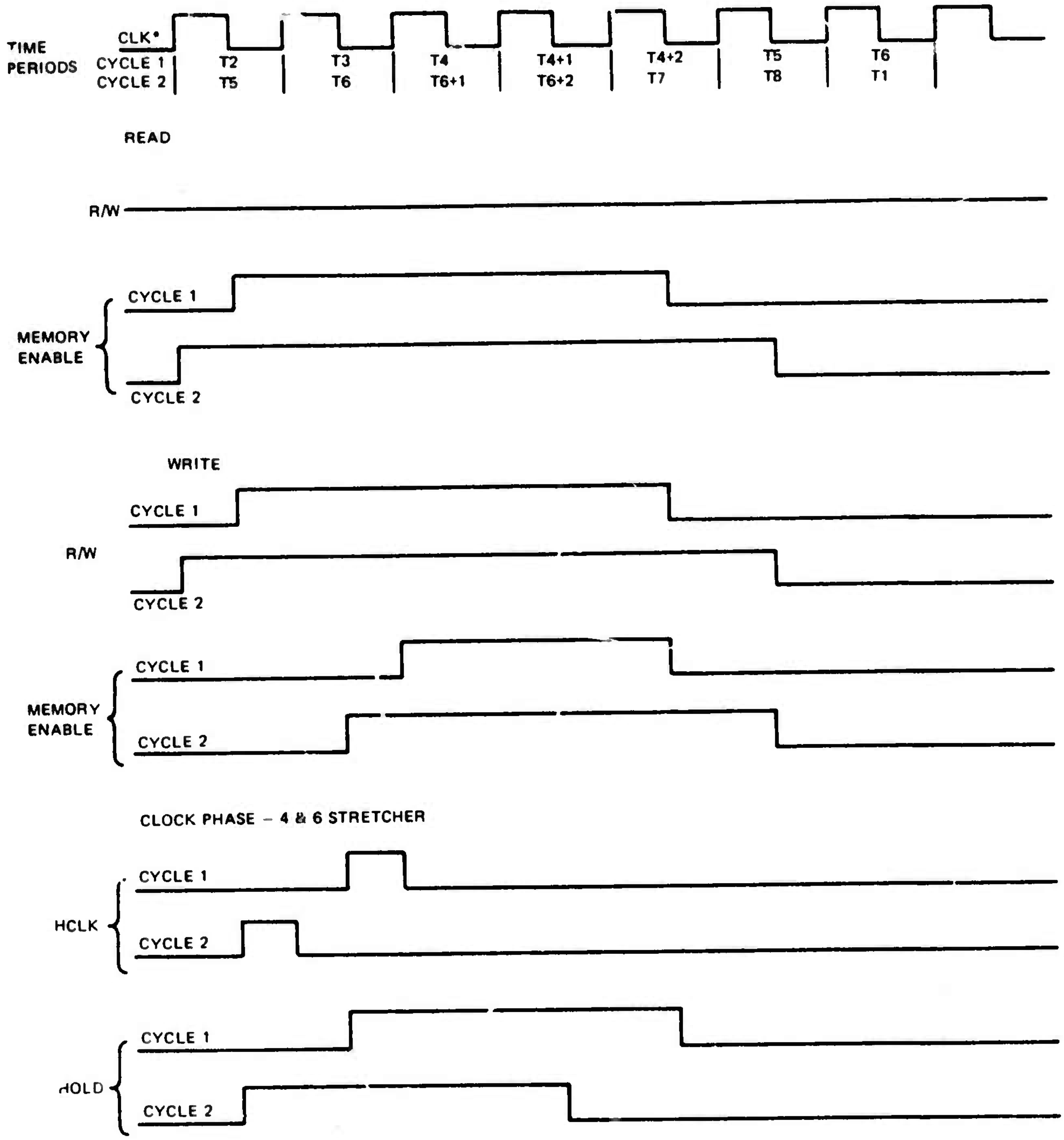


Figure 8.4-16. Read/Write Control Timing.

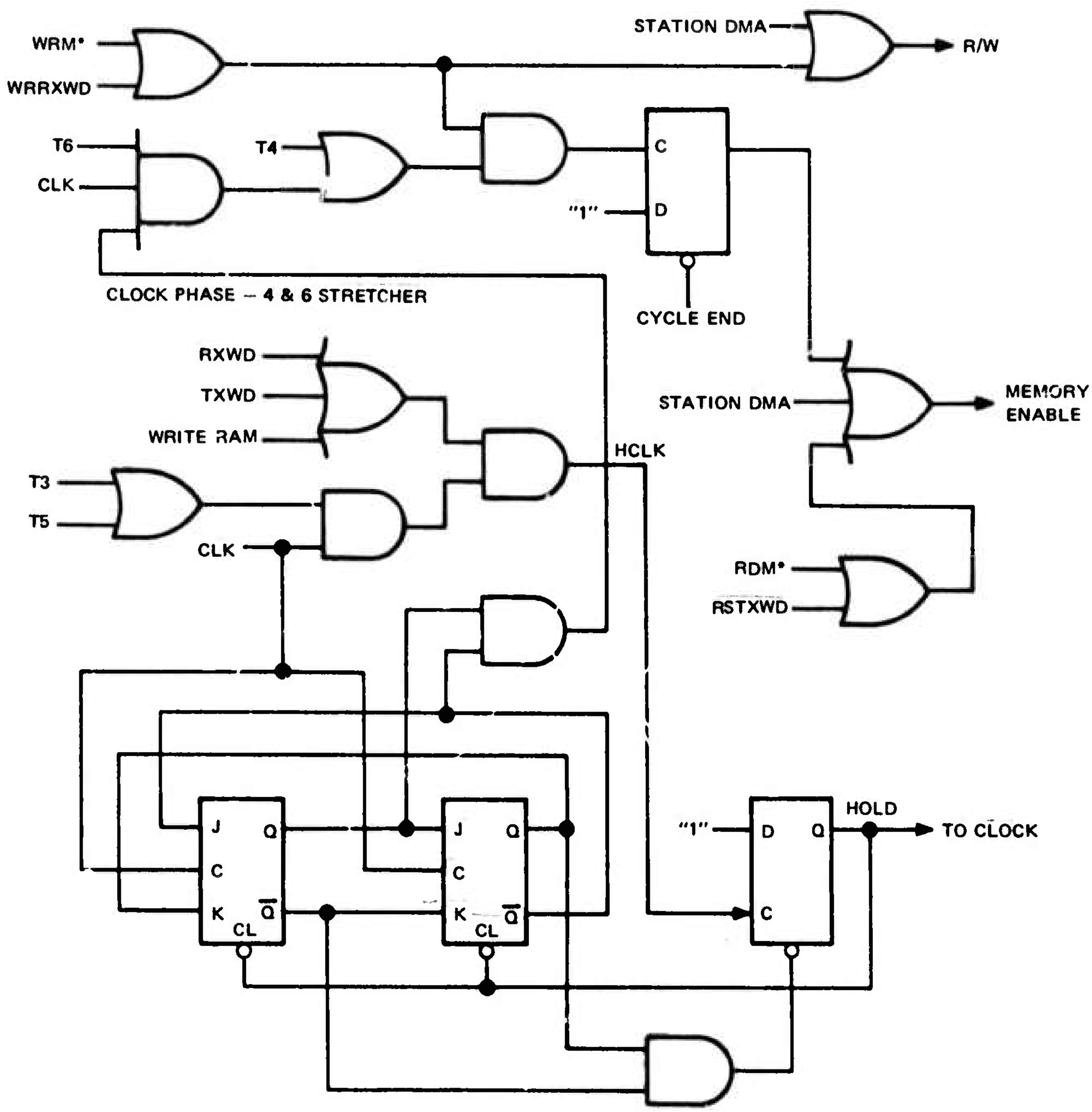


Figure 8.4-17. Read/Write Control.

8.4.6 I/O Channels

Two types of I/O channels are defined for the repeater microprocessor. These are the word transfer interface, as would be used in the terminal application, and the block transfer interface which would be used in the station application.

Each application requires implementation using interface hardware. This interface hardware is not included as a part of the repeater. However, provisions are made for adding the hardware on a modular basis external to the repeater. To this end, the signal interfaces are defined and an operating procedure proposed.

8.4.6.1 Terminal Interface

Figure 8.4-18 shows in block diagram form how an I/O device such as a tty is connected to the microprocessor. The interface signals are defined in paragraph 8.2. Figure 8.4-19 shows the block transfer DMA station application.

The I/O device can initiate a data transfer to the processor by raising the Interrupt Request line. The processor will identify the interrupting device by raising the Interrupt Select Status control flag. This flag will cause the device to put a bit on the data bus. This bit will correlate by software to a device address and the ahndler routine for that device. The processor will then raise the decoded address for that device and take a word of data from the data bus into the CPU.

This procedure will continue until the message is complete or until a packet buffer is filled. The processor will then transmit the packet.

In the receive mode, the processor will raise the device address line and strobe the data into the device data latch using the WRP control flag.

8.4.6.2 Block Transfer DMA - Station Application

The station requests a block data transfer of the microprocessor memory by raising the interrupt request line. This signal goes to a separate interrupt level input to the microprocessor that allows identifying the address of the station. The microprocessor will respond to the interrupt request by doing a read in (RIN) instruction, and taking a station word from the data buss. This status word will define to the software what service is requested by the station; i.e., read from memory or write to memory.

The microprocessor will initialize the DMA channel by setting up the memory starting address, loading the down counter, etc. The microprocessor will then HALT. The halt line will signal to the DMA channel and station processor that the data transfer can occur The DMA channel will step through the memory address and transfer the block of data.

When the transfer is complete, the DMA channel will raise the signal START, which will restart the microprocessor.

A block diagram of this application is shown in figure 8.4-19. The interface signals are defined in Section 8.2.

8.4.7 Software Organization

The system operating programs for the repeater, terminal, and station will be stored in non-volatile memory (PROM). These operating programs will not be identical for the various applications, but there will be many similarities. Key parameters required by the program to be stored in RAM will be generated by the system program during the power-up procedure. Network parameters such as routing, labels, etc., will be stored in RAM during initialization.

The processor organization is patterned after the National Semiconductor IMP-16C. The design intent has been to retain the entire 60 OP-CODE instruction set available in the IMP-16C without placing any additional constraints on the programmer. To the extent that this organization has been defined, no operational situations have been identified to prevent this objective. The instruction set is implemented by the use of a microprogram stored in a control read only memory.

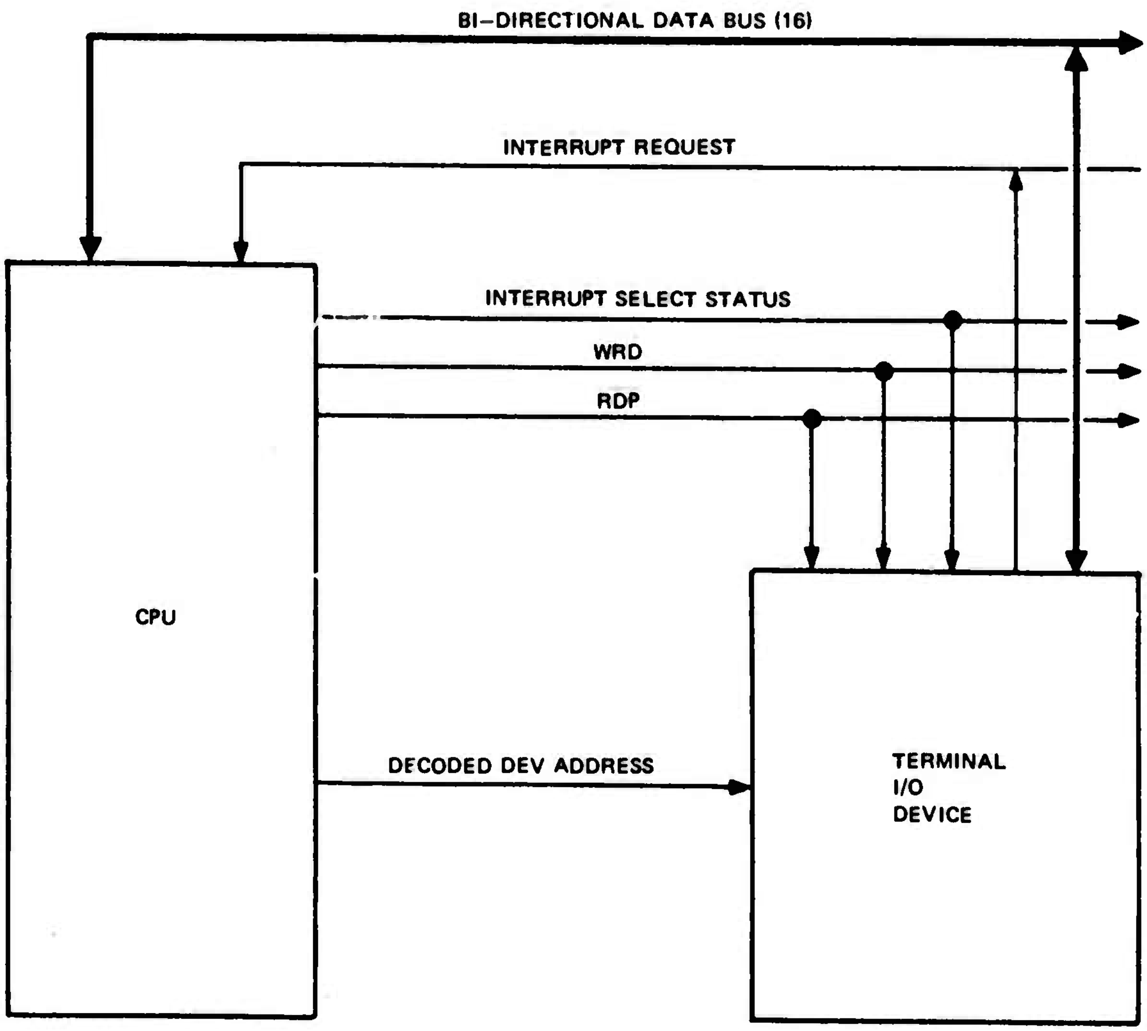


Figure 8.4-18. Terminal I/O Interface.

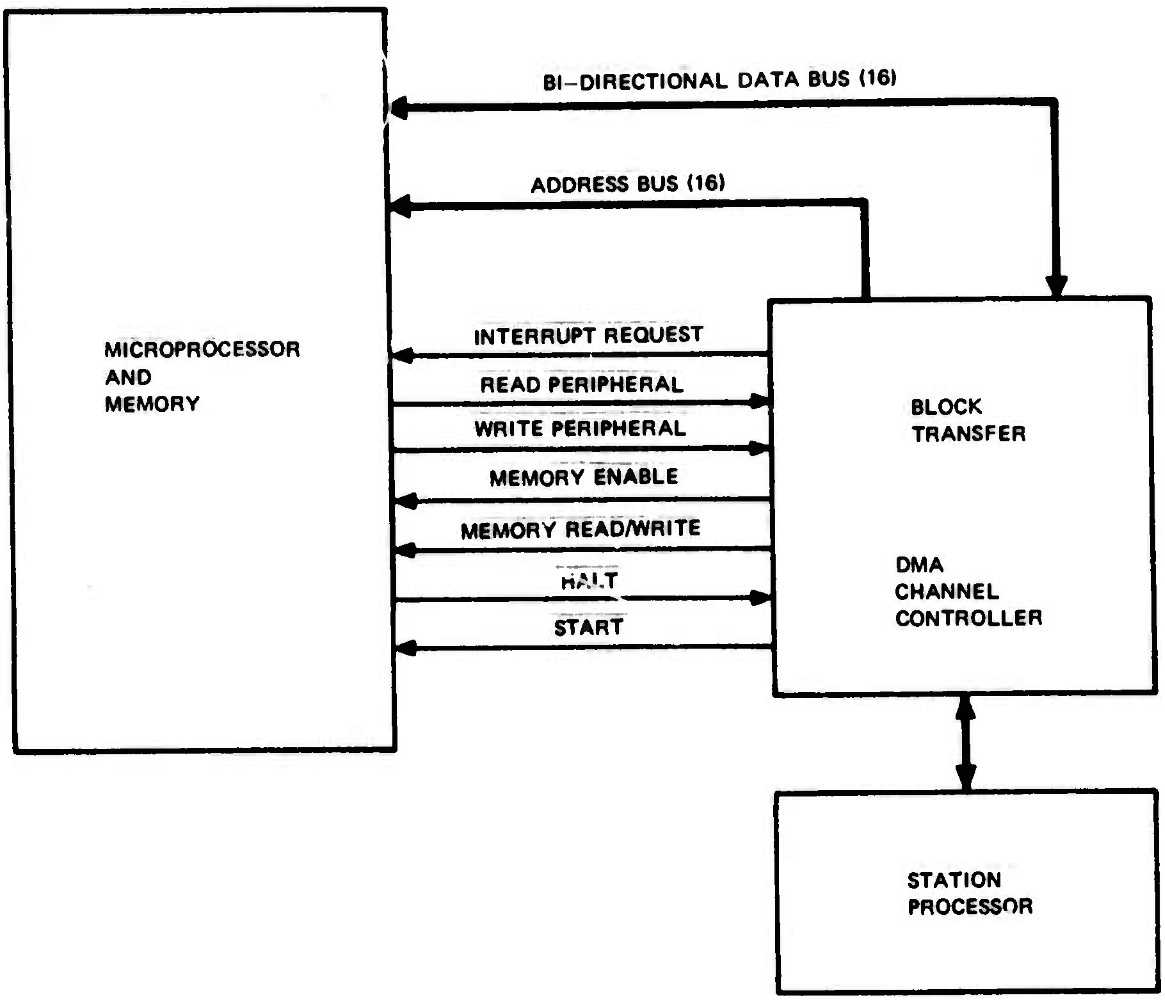


Figure 8.4-19. Block Transfer DMA Station Application.

The operating software will include the following major functions:

Initialization. Includes local initialization during power-up sequencing and network initialization by communicating with the station.

Packet Handling. The packet in/packet out discipline established by the network operating structure. This includes handling of errors, routing and addresses, acknowledgment schemes, etc.

Device I/O. For terminal and station applications where the repeater hardware is used as a front end packet handler, and other hardware and software is involved in the operation.

Performance Monitoring. Special software used in the experimental environment for gathering performance data for verification of system models.

Software Development Aids

Several aids are available for use in the prototyping units for developing the system programs. Some of the more useful tools are:

Assembler. A resident assembler and a cross assembler are provided.

Loader. A loader is available for entering programs produced by the assembler into read/write memory.

Program Debug Aid. A program that provides aids for troubleshooting program development.

Diagnostic Programs. A program for testing and verifying operation of the central processing unit and the memory.

8.5 COMMUNICATION SECURITY

In order to include communication security in the design plan, the following assumptions are made:

END-TO-END ENCRYPTION/DECIPHER. Therefore, the COMSEC problem becomes one for stations and terminals.

PACKET HEADER IS PASSED CLEAR. A repeater handles secure data as it would any plain packet.

COMMUNICATION SECURITY BASED ON PRIVACY ONLY.

ENCRYPTION AND DECIPHER ARE DONE OFF-LINE AT STATIONS AND TERMINALS.

An overview block diagram of a terminal COMSEC location is shown in figure 8.5-1.

For the operational sequence given, the packet is assumed to have the following information CLEAR in the header:

Originating ID

Prep Code (Date/Time)

Cipher/Plain Bit

Terminal Address

An operational sequence would typically go as follows:

Send

- Operator sends date/time. Processor forwards date/time. COMSEC preps.
- Operator enters CALLED address. COMSEC passes in clear. Processor inserts in header.
- Operator enters message - character serial. COMSEC encrypts and hands to processor a word at a time. COMSEC handles interrupt and data transfer.

  Processor outputs data to modem via the packet DMA in the normal manner.

Receive

- Packet arrives. Modem enters packet to memory using packet DMA in the normal manner.

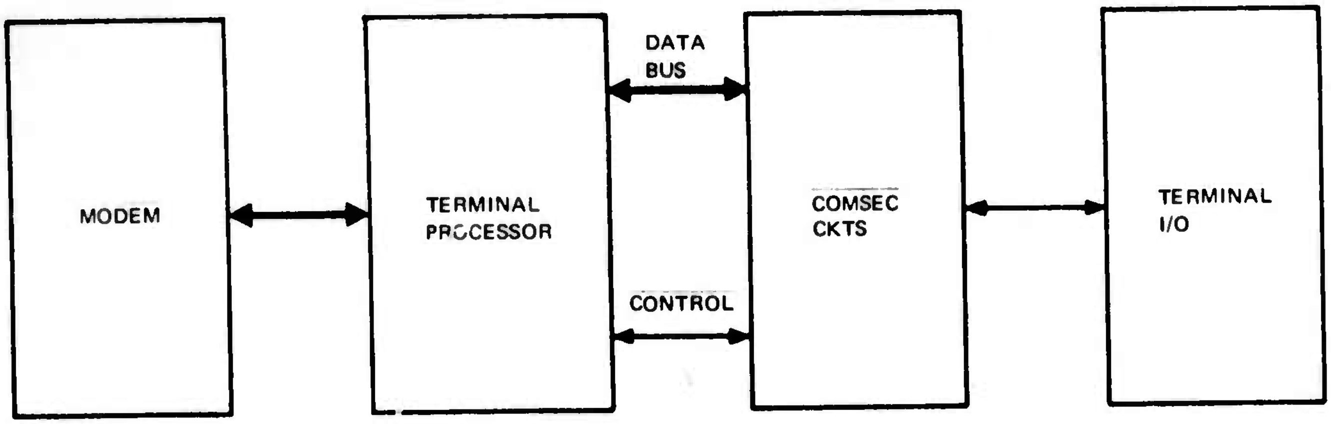


Figure 8.5-1. Terminal COMSEC Location.

- Processor hands date/time to COMSEC. COMSEC preps.
- Processor hands packet to COMSEC - word serial. COMSEC deciphers and hands word serial to I/O device.

8.6 PROTOTYPE REPEATER CONFIGURATION

The repeater (excluding power) is packaged in a pole mounted weatherproof container. The high gain antenna mounts directly to the top of the cabinet. The repeater is the easiest to define physically at this time since it is not complicated with unknown I/O devices and crypto.

8.6.1 Capability Summary

The repeater is designed for two data rates; 100 kBps and 420 kBps. Each rate requires its own SAWDS, amplifiers, and detectors.

For optional multiple detectors (time displaced codes), the output from the SAWDS can be split to operate separate coherent agc amplifiers and set at sync, preamble, and data detectors.

8.6.2 Composite Diagram

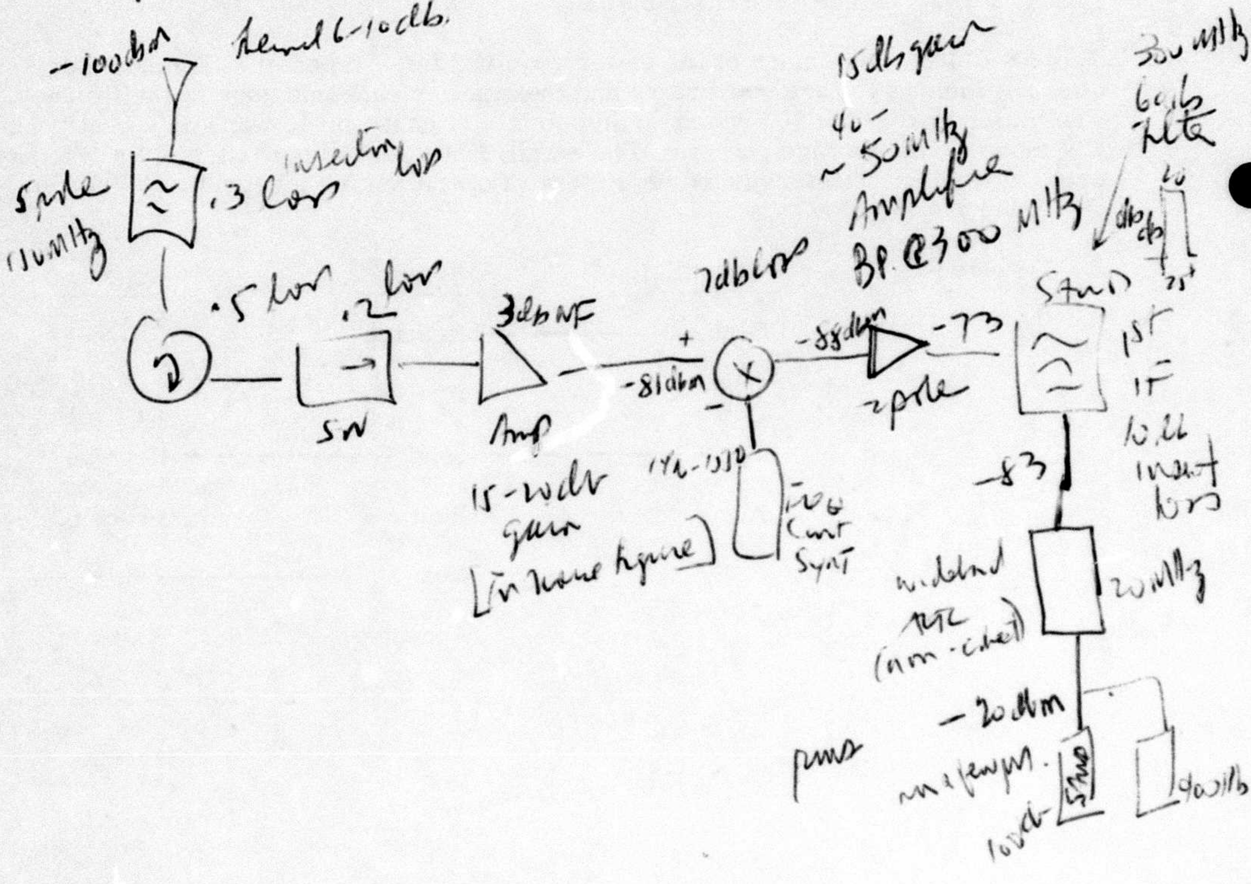
Figure 8.6-1 shows the composite diagram for the repeater.

8.6.3 Power Sources and Distribution

Table 8.6-1 is a summary of the power required for a repeater. The summary does not include voltage converters and their power consumed due to inefficiency. The major load is the PA which could potentially consume 45 watts in a continuous CW mode. The average power will be significantly less, approximately a 1/6 duty cycle assuming the following normal network operation for a repeater.

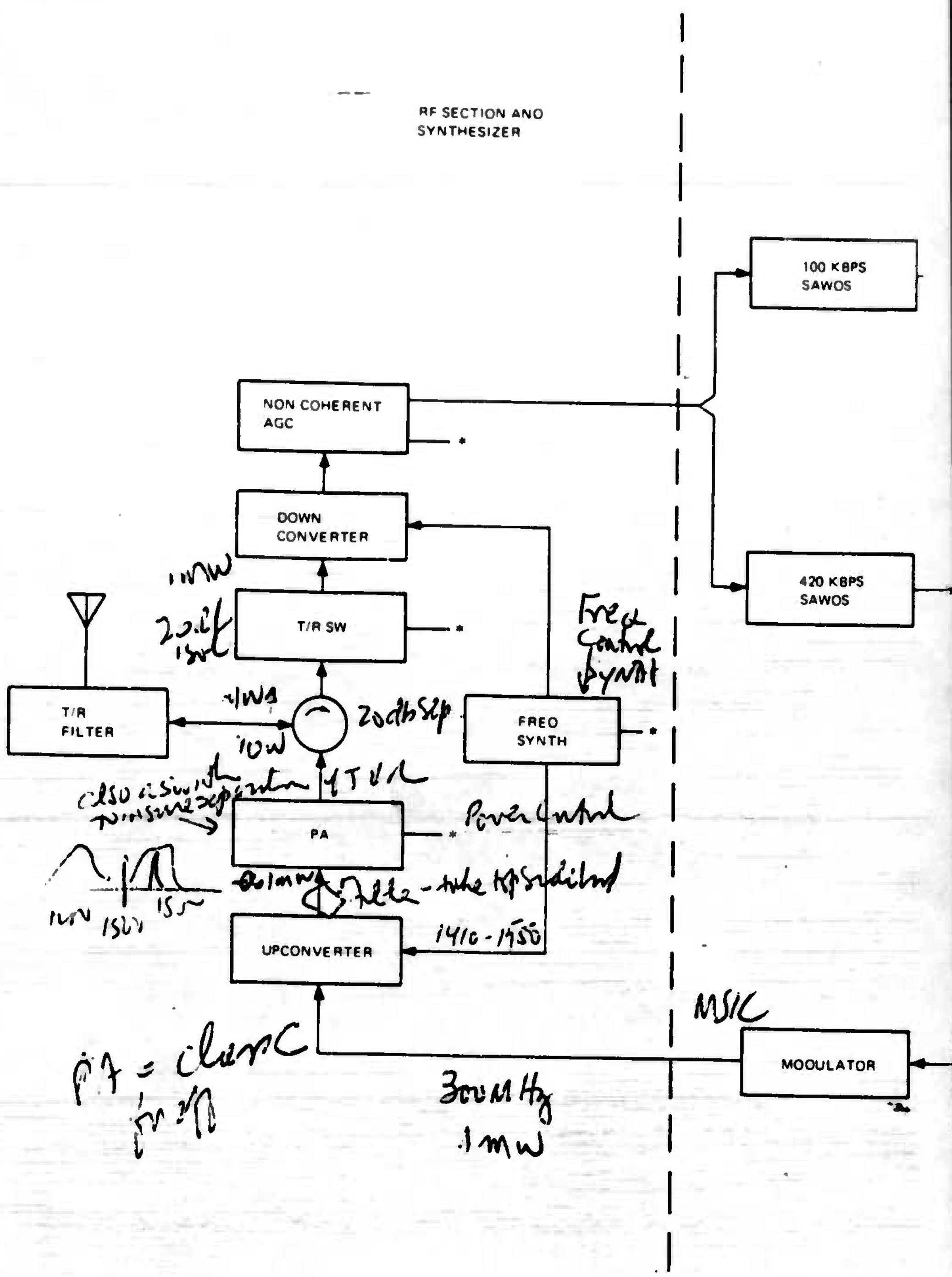
Packet Period	Terminal	Repeater	Repeater
1	Send →	Receive	
2	Wait	Process	
3	Echo ←	Send →	Receive
4	Accept	Wait	Process
5		Echo ←	Send →
6		Accept	Wait
7			Echo
8			[illegible]ept

Rec



-100dbm
5pole
110MHz
.3 loss
insertion loss
.5 loss
.2 loss
SW
3db NF
Amp
15-20db gain
[in noise figure]
-81dbm
7db loss
Freq Cont Synt
-88dbm
15db gain
40-50MHz
Amplifier
BP @ 300 MHz
2pole
-73
300 MHz
6db
Filter
1st IF
10db insert loss
-83
20MHz
wideband
-20dbm

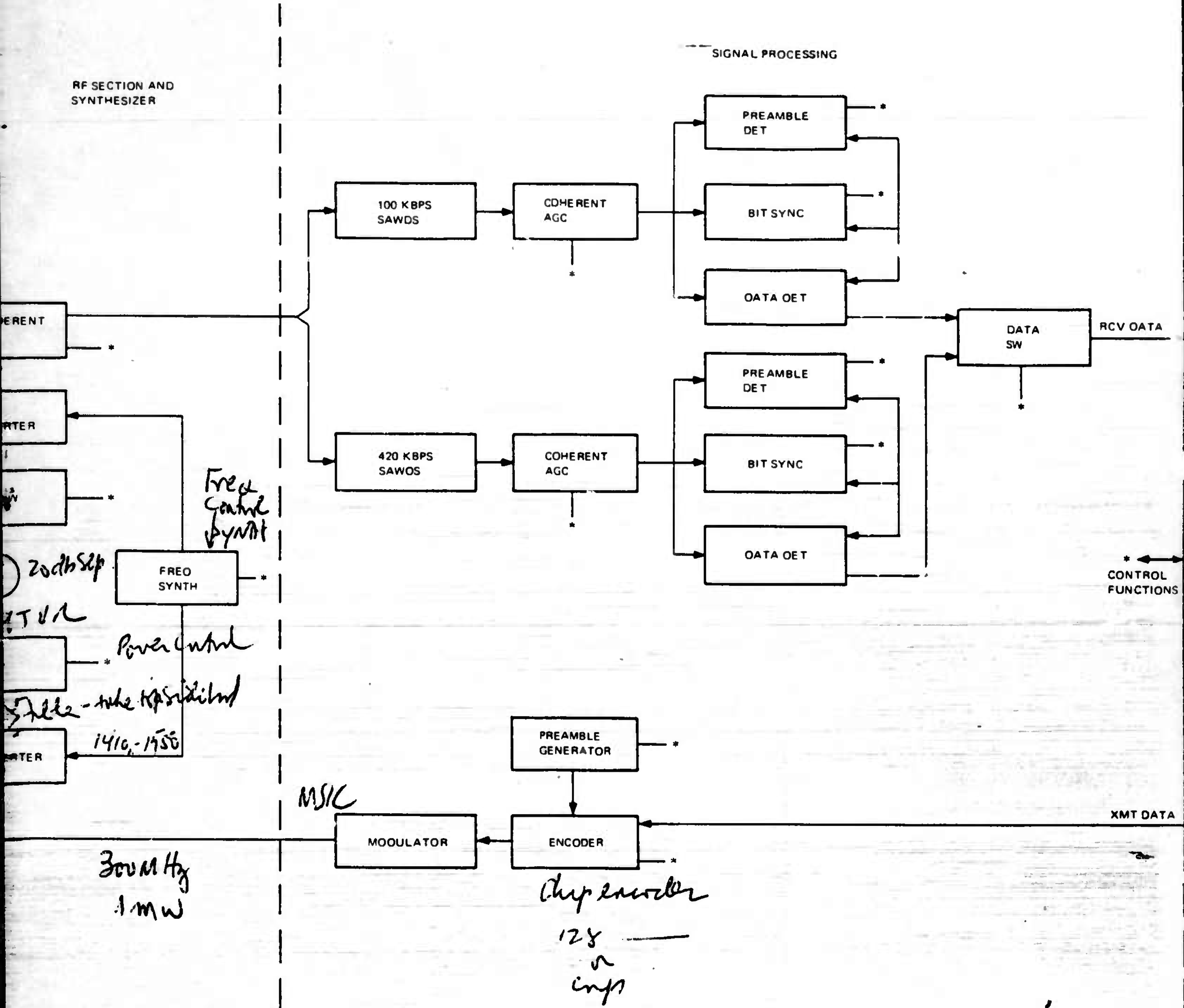
RF SECTION AND
SYNTHESIZER



NOTES

* INDICATES CONTROL FUNCTIONS

10f3



NOTES

* INDICATES CONTROL FUNCTIONS

2 of 3

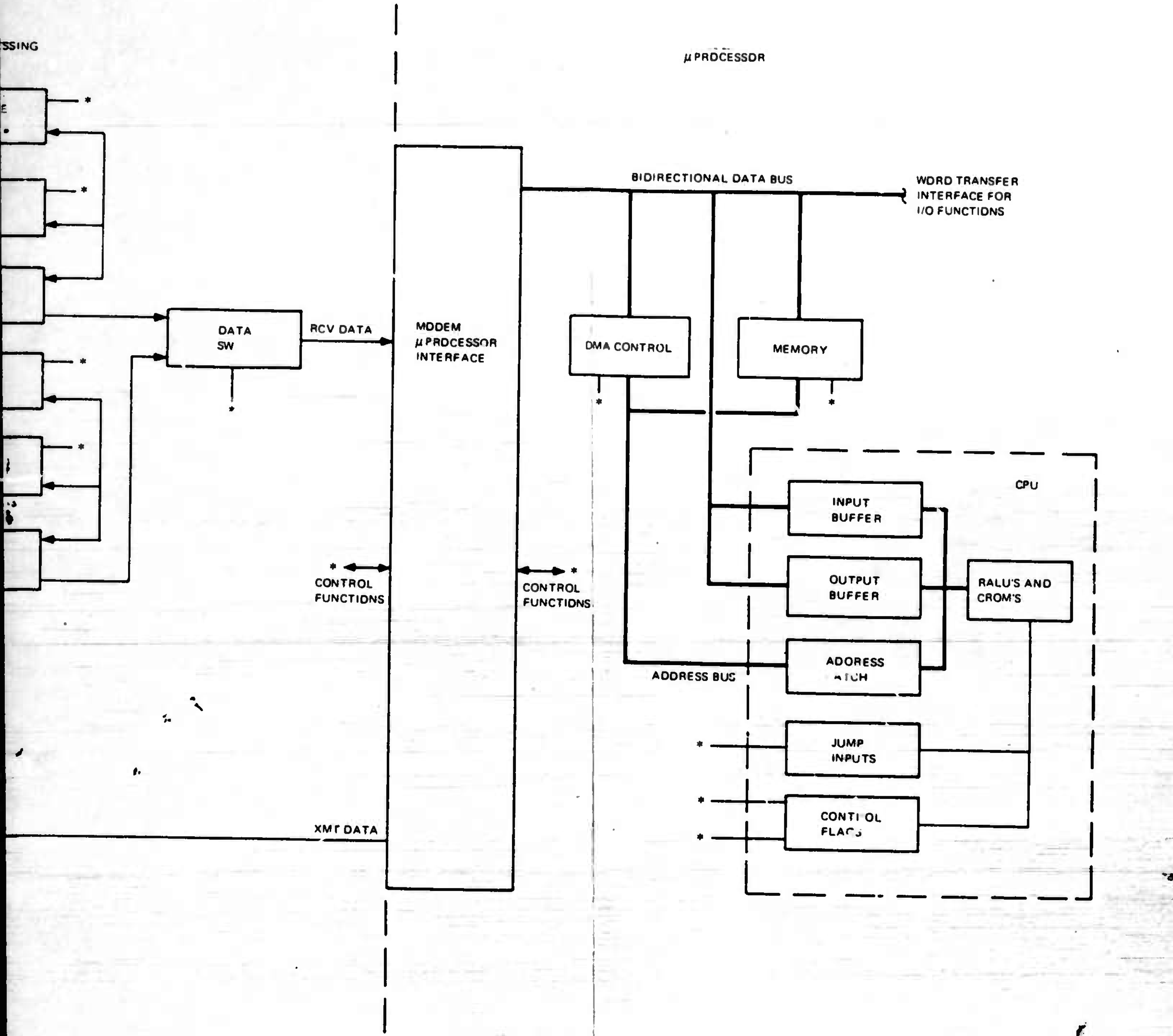


Figure 8.6-1. Repeater Composite Diagram.

3 of 3

Table 8.6-1. Power Consumed by Equipment.

SUBSYSTEM	CURRENT IN/AMPS PER VOLTAGE						POWER IN WATTS FOR SUBSYSTEMS
	+24V	+15	+12	+5	-5	-12	
RF (10W CW PA)							
PA	0.01 + 1.9 (XMT %)*						0.240 + 45 (XMT %)
Up-Converter and Control		0.020					0.300
Down-Converter		0.020					0.300
T/R SW				0.02 + 0.02 (XMT %)			0.100 + 0.1 (XMT %)
Subtotal	0.01 + 1.9 (XMT %)	0.040		0.02 + 0.02 (XMT %)			0.940 + 45.1 (XMT %)
SYNTHESIZER							
Frequency Synthesizer		0.130		0.210	0.240		4.23
COMMON RADIO MODULES (Used for all bit rates)							
Preamble and Code Gen				0.064			0.320
Modulator			0.020		0.020		0.340
IF. AGC Ampl			0.062		0.012		0.810
Subtotal			0.082	0.064	0.032		1.464

*XMT % = XMT DUTY CYCLE

Table 8.6-1. Power Consumed by Equipment (Cont).

SUBSYSTEM	CURRENT IN/AMPS PER VOLTAGE						POWER IN WATTS FOR SUBSYSTEMS
	+24V	+15	+12	+5	-5	-12	
MODULES PECULIAR TO BIT RATE OR DETECTOR							
Coherent AGC & Det			0.132		0.020		1.700
Preamble Det				0.036	0.030		0.330
Bit Sync		0.080		0.076	0.053		0.765
Data Det			0.016	0.020		0.020	0.525
Per Data Rate		0.080	0.148	0.132	0.103	0.020	4.39
Sub-Total (2 Rates)		0.160	0.296	0.264	0 203	0.040	8.78
MICROPROCESSOR							
μ Processor				1.120		0.260	8.720
TOTAL CURRENT AND POWER SUMMARY							
Repeater Total Current	0.01 + 1.9 (XMT %)	0.330	0.378	1.678 + 0.02 (XMT %)	0.478	0.300	
Total Power	0.24 + 45 (XMT %)	4.95	4.536	8.39 + 0.1 (XMT %)	2.39	8.6	24.11 + 45.1 (XMT %)
*XMT % = XMT DUTY CYCLE							

If the echo acknowledge is not received, then the repeater will retransmit causing a 1/3 duty cycle of: Send/Wait/No Echo/Retransmit.

The greatest power surges are thus for the PA. For this reason, a primary power source voltage of +24 Vdc is proposed for the equipment since this is what the PA requires. If the system were powered from an external 24-volt primary power source, the PA could be operated directly on the primary power. A drop in battery voltage with time would cause the output power to decrease but only a few dB (see appendix C.5). The power lost by dc to dc converters is thus avoided which will extend battery life. From table 8.6-1, the net power required for a repeater which includes the microprocessor, a 10W PA and a 100-kBps and 420-mBps modem but excluding the dc to dc converters is: 24.11 + 45.1 (XMT Duty Cycle) watts.

It should be noted that the design of the component functions of the radio and microprocessor has stressed low power consumption. Low power TTL and CMOS devices have to be used where possible. ECL devices which require considerable power have been used only where necessary. The possibility of the equipment every becoming truly mobile requires careful consideration of design to reduce power consumption. It would be easy to build a 20-pound, 1-cubic foot repeater that might require several tons of batteries to make it operate for a few months. Multiple batteries to supply the voltage was considered impractical. Twenty-four volts is a standard voltage easily obtained by many means whereas the other voltages (±15V and ±5V) are not. Thus, the use of the single 24-volt dc source is selected. The dc to dc converters will be used to develop the voltages from 24V.

Standard integrated circuit regulators are inexpensive and small. They are, however, of the series pass element type. The efficiency of this type of regulator rarely exceeds 50 percent and usually is considerably lower. The dc to dc converters can be made using switching regulators or pulse width modulated regulators that have between 60- and 80-percent efficiency. The design is usually based on a well defined load and supply voltage. Since this is still an experimental system, the load could change as the design progresses or design requirements change. A common power supply would usually be over- or underrated. Any growth, as might be the case for multiple detectors or other operating schemes, would require redesign of the power system.

For preliminary planning purposes, a central modular power supply is proposed. A 24V source will drive a high efficiency switching converter. The converter output is then supplied to voltage regulators that are high efficiency switching regulators to provide the desired voltage levels. As requirements change, only those building blocks of the power supply need be changed to satisfy the requirement.

Figure 8.6-2 is a block diagram of the repeater power supply being proposed as a low risk solution. The figure also shows the projected efficiency and the power input.

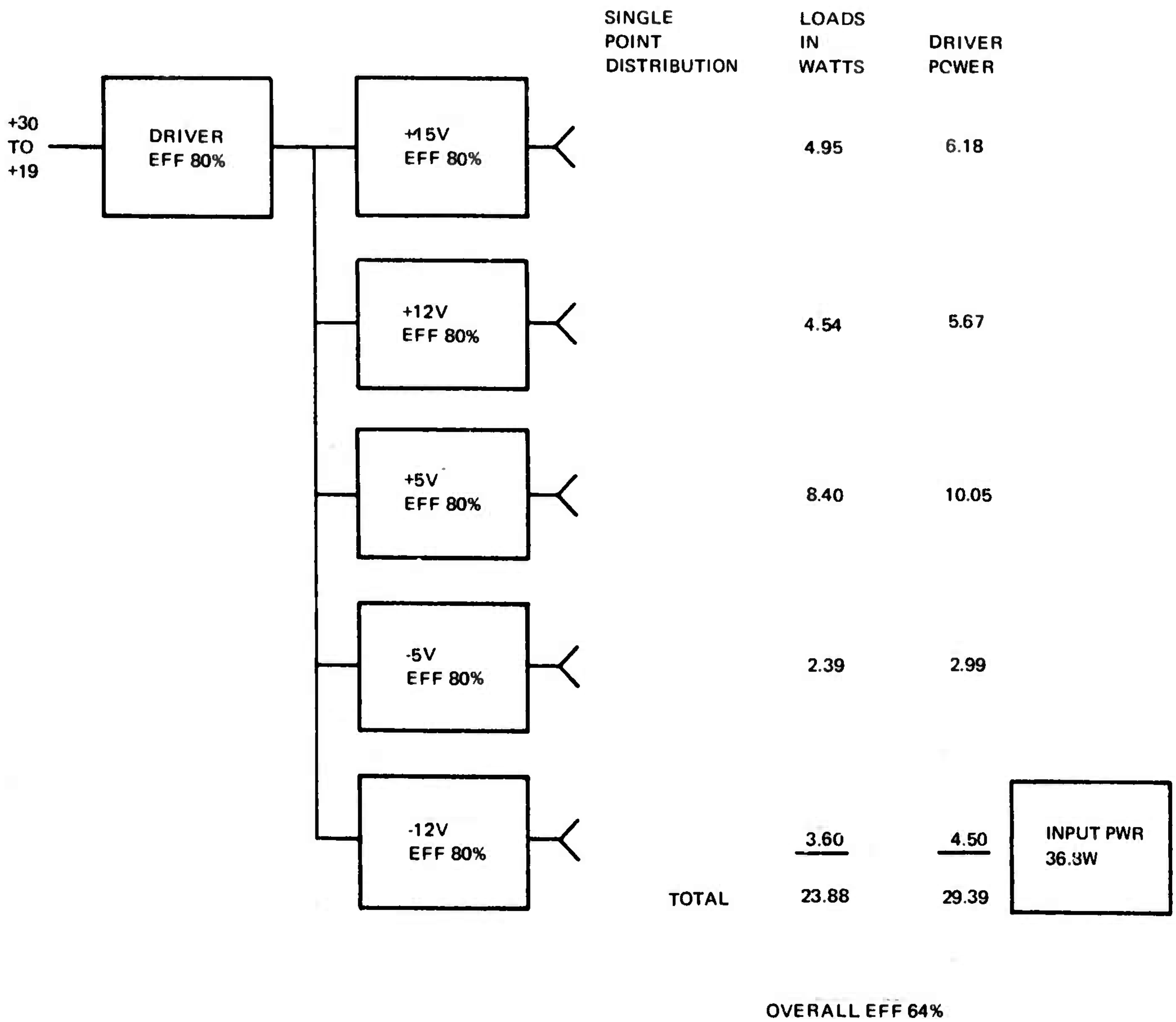


Figure 8.6-2. Repeater Power System (Excluding 24 Volts).

The total power required for the repeater is:

36.8W + 45 (XMT Duty Cycle)

% Duty Cycle	Total Input PWR (24V)
Receive	36.80 Watts
5	39.05
10	41.30
15	43.55
20	45.80
30	50.30
50	59.30

To put the power in perspective, if 1 ton of lead acid batteries are used, the repeater would operate for approximately 2 weeks. (This is obtained from figure 5 of appendix C.5. Extremely expensive silver Zinc batteries could be used and a reduction to 200 pounds of batteries would be required. The energy densities are approximately:

Lead Acid	10 WHR/lb
Silver Zinc	100 WHR/lb

The logical solution is to power the repeater from a thermoelectric generator if isolated unattended operation is required. If ac power is available, the use of a conventional ac to 24Vdc power supply is most logical.

8.6.4 Physical Description

The repeater unit which consists of the rf section, frequency generator, signal processor, digital section, and power supplies is packaged in a rugged, lightweight, drip-proof container. The package configuration is shown in figure 8.6-3. The rf head is mounted into the cover which is hinged to the main card cage type chassis. The cover has fins for efficient heat dissipation for the high powered rf transistors. The antenna mounts to the cover and may be detached and reverse mounted for convenient transportability. The cover also has a quick latching clamp for mounting the combined unit to a pole to elevate the unit for better reception.

The latches provide quick access to the O-ring sealed card cage containing the circuit cards and the hard mounted power supplies. Heat from the power supplies is conducted from the base to the side walls for efficient cooling. The estimated temperature rise for the unit is 12°C.

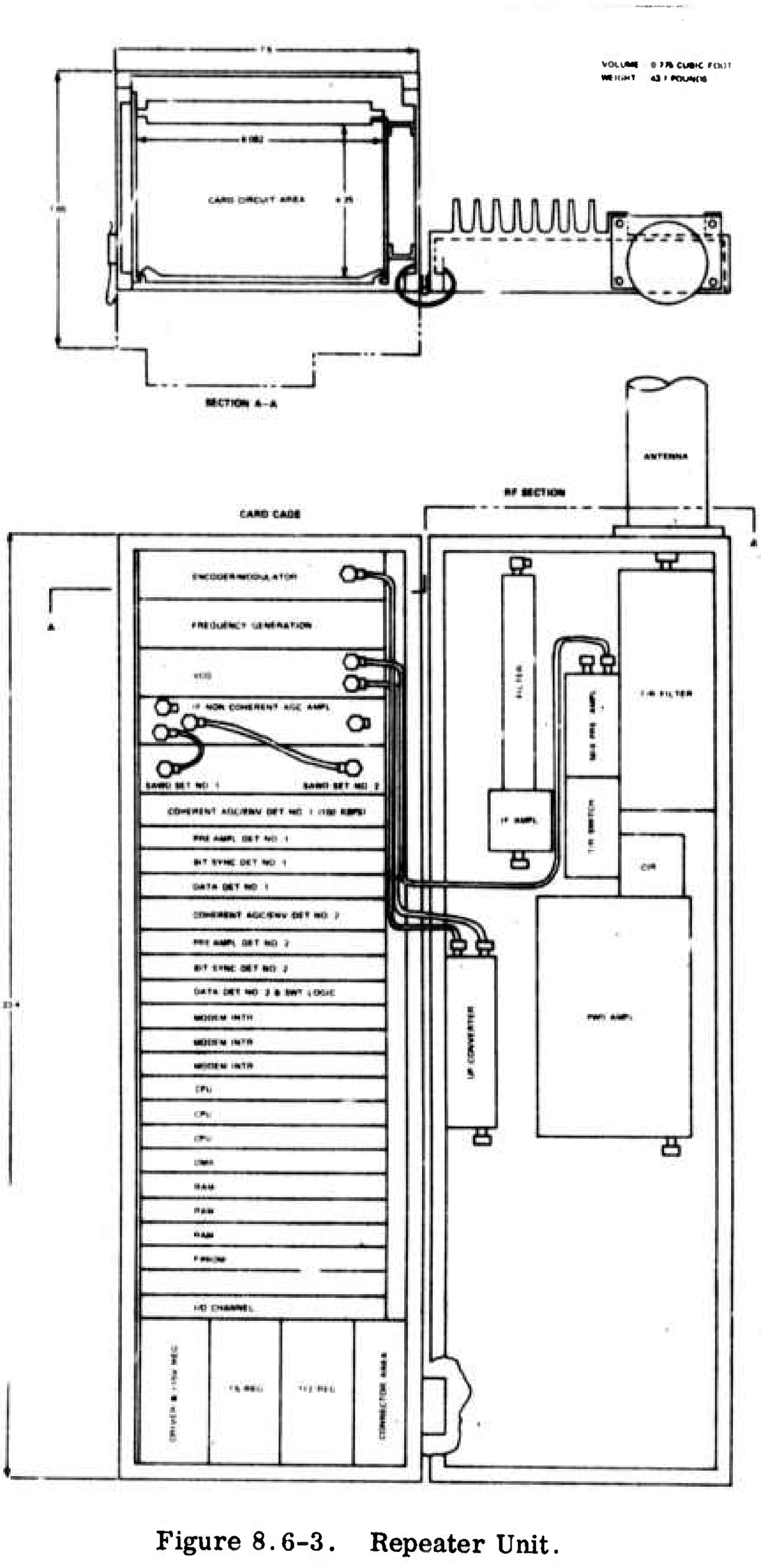


Figure 8.6-3. Repeater Unit.

The 6.062- x 4.25-inch circuit cards with a locking type handle which provides identification are used. The cards plug into edge-on wire wrap connectors. Future units will provide card interconnection via a printed circuit backplane and 0.25 square pin/socket type board contacts. A rear cover provides access to the wiring.

Optional Packaging

Several alternate packaging methods are possible in addition to the combined configuration described above. Table 8.6-2 lists the possible configurations, sizes, volume, and weights of each.

The repeater may be divided into two sections; the rf/antenna section and the card cage section. The rf section shown in figure 8.6-4 contains the high frequency components with the up and down converters to reduce the signals to an acceptable form to transmit to the signal processing equipment in the card cage. The lightweight unit is easily placed in an elevated location. Mounting clamps are provided for securing to a pole. The modified card cage section is similar to the basic unit shown in figure 8.6-3 except that the rf section is replaced with a cover similar to the rear access cover. This unit could be located at the base of a mounting pole allowing easy test and maintenance. An alternate card cage section is shown in figure 8.6-5.

8.6-5. Maintenance and Self Check

Since the repeater is for unattended operation, vital performance levels must be determined, monitored, and supplied to the microprocessor. The data would periodically be transmitted to the station for monitor and preventive maintenance. Critical thresholds will be established that would preempt normal traffic to send a packet indicating a major problem. Some of the vital signs might be:

- Battery or Primary Power Status
- XMTR rf output power
- Signal and power levels within repeater.

In addition to the maintenance of the equipment, there are network parameters that are desirable to report. These parameters might be:

- Such measures as retransmission required,
- Traffic Statistics, etc.

The above considerations are not firm and require further evaluation from a network operation viewpoint before implementation.

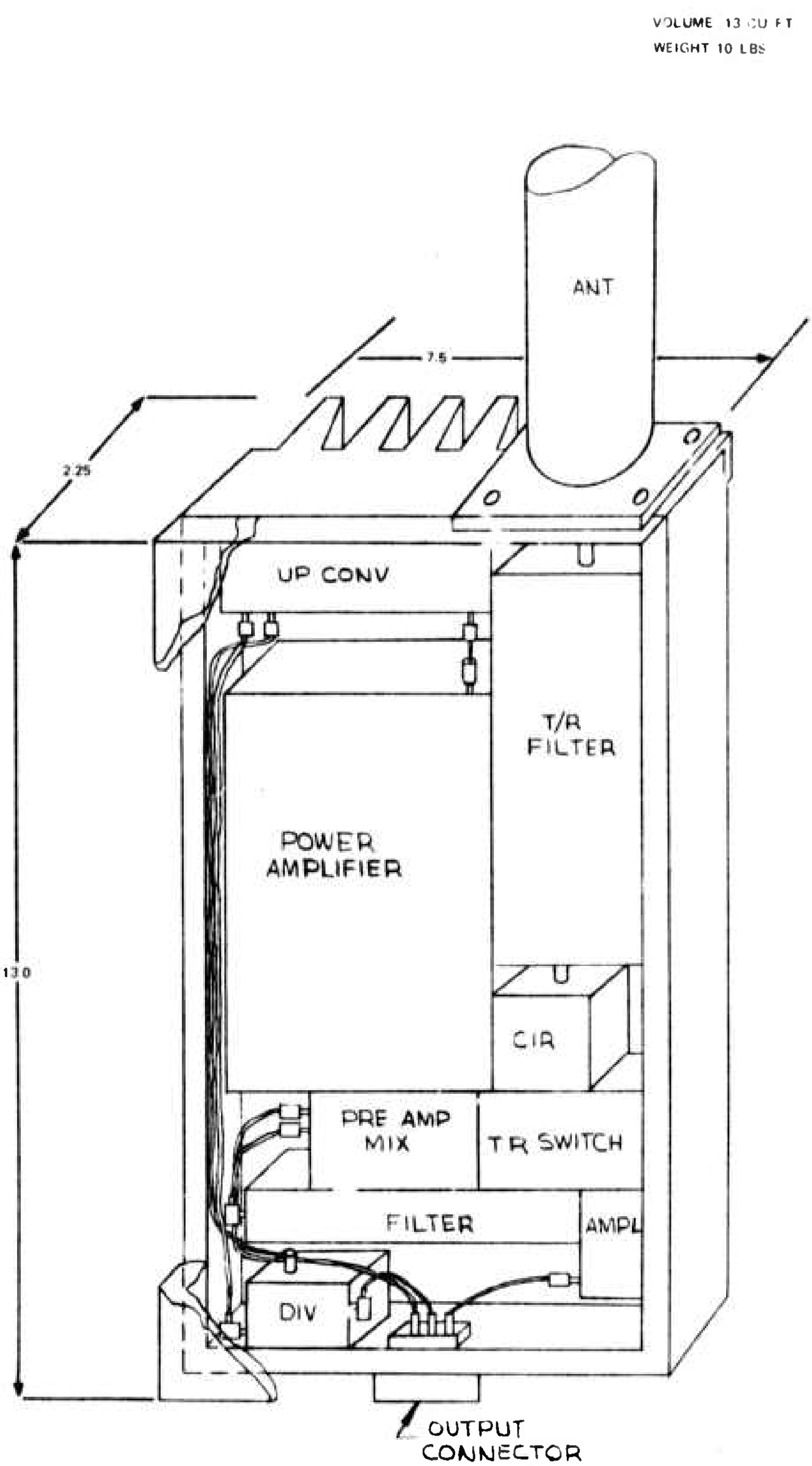


Figure 8.6-4. RF/Antenna Section.

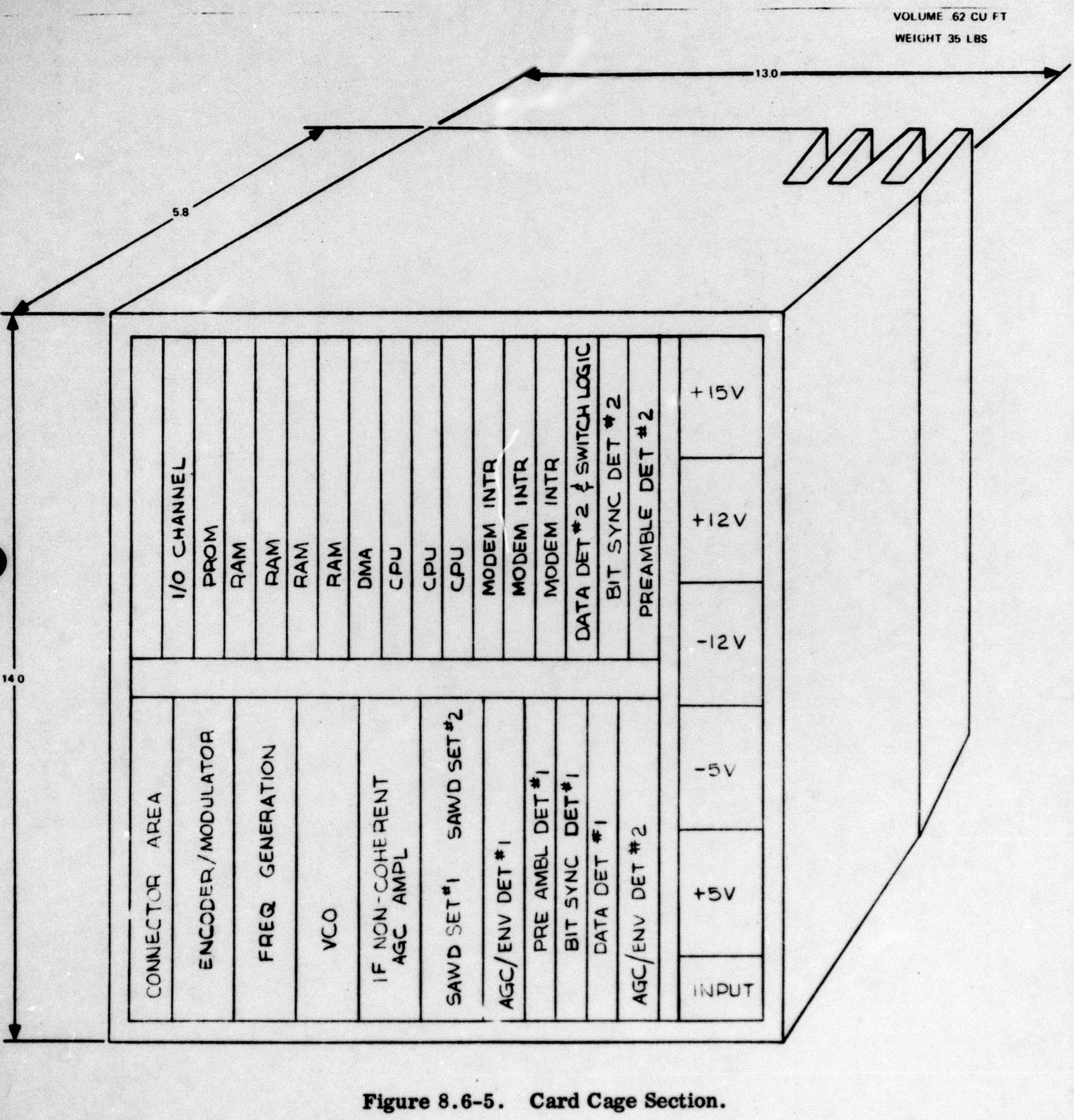


Figure 8.6-5. Card Cage Section.

Table 8.6-2. Physical Repeater Statistics.

	FIGURE	SIZE (INCHES)	VOLUME (CU FT)	WEIGHT (LBS)
Repeater				
Basic Unit	8.6.4A	7.5 x 7.65 x 23.4	0.775	43.7
Divided Unit				
RF Section	8.6.4B	7.5 x 2.25 x 13.0	0.13	10.0
Card Cage Section A	8.6.4A	7.5 x 5.8 x 23.4	0.55	34.0
Card Cage Section B	8.6.4C	5.8 x 13 x 14	0.62	35.4

8.7 PROTOTYPE TERMINAL CONFIGURATION

The I/O devices for the terminal are not completely defined at this point as to required capability, size, weight, and power consumption. To allow flexibility, the I/O device interface will be designed per RS-232-C. This allows off-the-shelf equipments to be interconnected. Not included at this time are the crypto interfaces and characteristics.

8.7.1 Capabilities Summary

As a matter of convenience and interchangeability, the prototype terminal signal processing section will include both data rates, allowing the unit to act as a repeater if properly programmed. This would allow more flexibility during the evaluation period. The terminal complement with conventional I/O devices will at best be a suitcase size unit. The intention at this point is not to microminiaturize the terminal.

8.7.2 Composite Diagram

Figure 8.7-1 shows the major system interconnect.

8.7.3 Power Sources and Distribution

Without duplicating what was said for the repeater, it is important to repeat that power consumption is a serious problem, if the equipment is ever to be truly portable. By having the terminal radio the same as a repeater in its prototype configuration, its power will be the same as a repeater. The I/O interface and I/O devices could require an additional 120 watts while printing.

The power scheme for the terminal is based on a 24-volt dc primary power source for all equipment. Initially, an ac/dc supply could be used and later a battery pack could be provided to support short term portable operations. The power supply or battery pack would be a separate portable item allowing maximum flexibility of selecting the power source for the intended application and situation. Appendix C.5 addresses battery size and weight considerations as a function of power drain and duration of operation that could be expected.

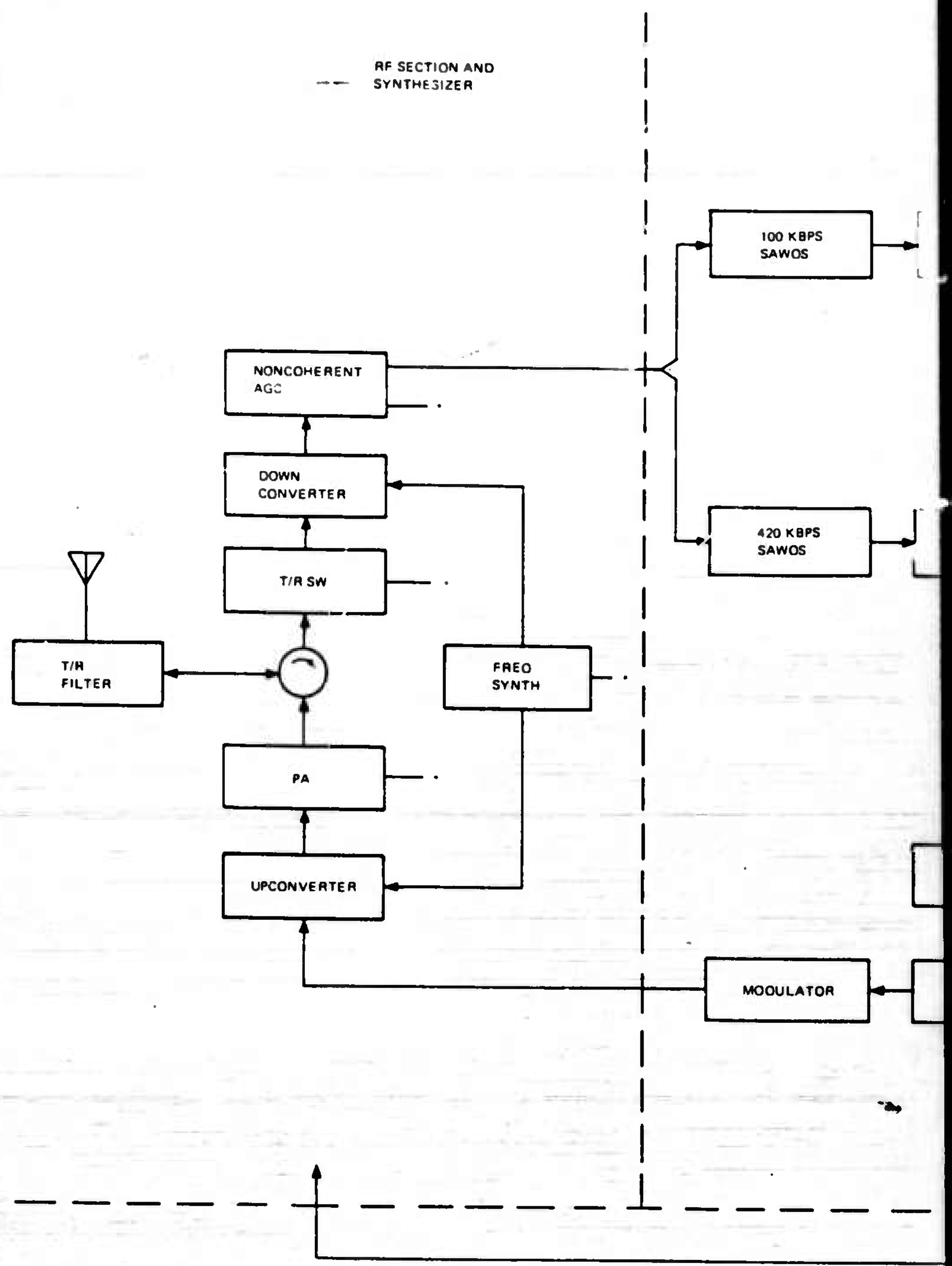
No attempt is made at this time to define the total power required and any portable power source.

8.7.4 Physical Description

Suitcase configuration with companion power pack suitcase. To be defined later.

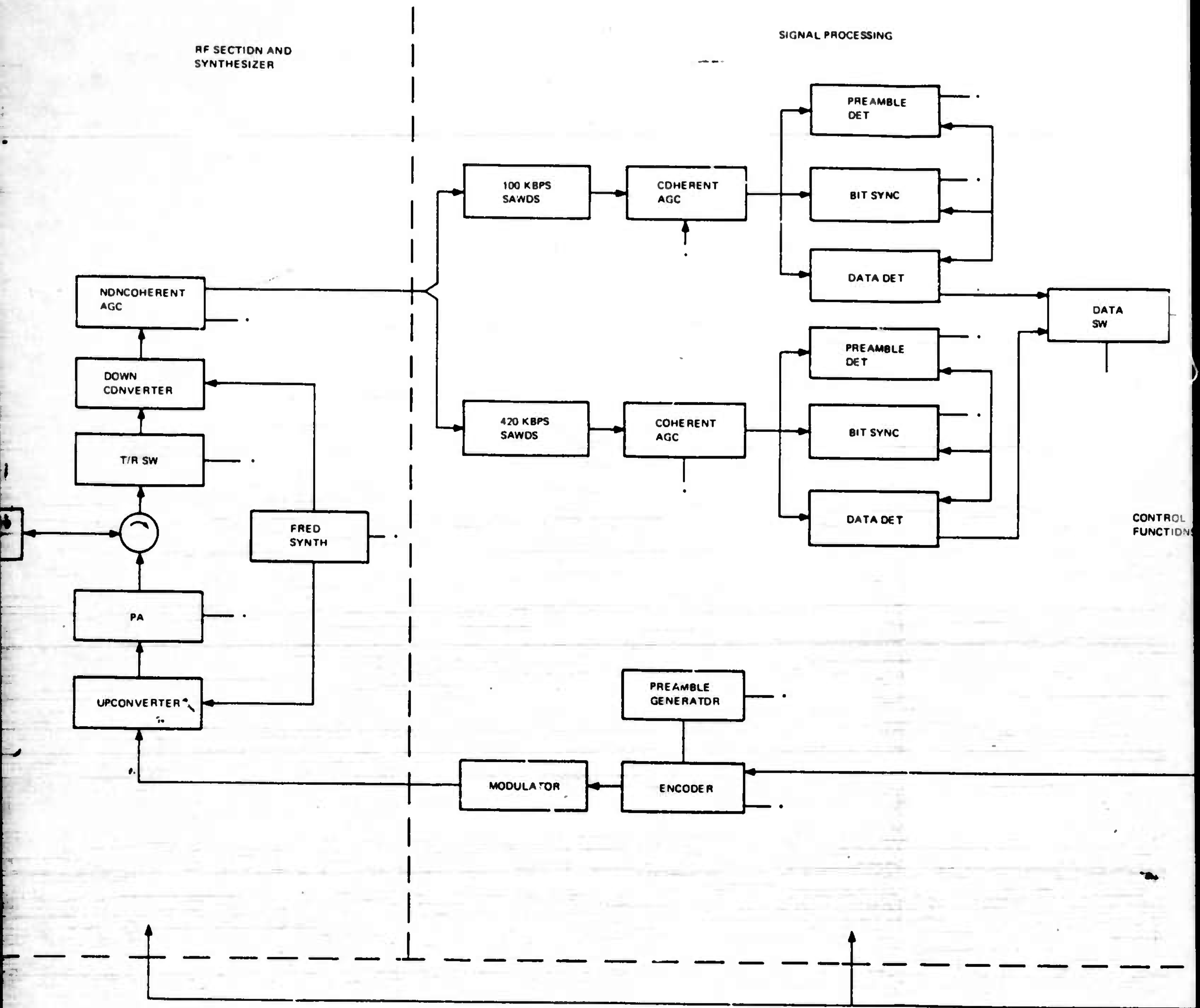
8.7.5 Maintenance and Self Check

It is essential that the TCU's provide capacity for terminal and repeater link testing and that the user be provided with simple mechanisms for checking the terminal-to-TCU-to-repeater functions. This includes, but is not limited to sense lights, loop tests, and standardized messages for testing network response.



RF SECTION AND SYNTHESIZER
100 KBPS SAWOS
NONCOHERENT AGC
DOWN CONVERTER
420 KBPS SAWOS
T/R SW
T/R FILTER
FREQ SYNTH
PA
UPCONVERTER
MODULATOR

1 of 3


RF SECTION AND
SYNTHESIZER
SIGNAL PROCESSING
PREAMBLE
DET
100 KBPS
SAWDS
COHERENT
AGC
BIT SYNC
DATA DET
NONCOHERENT
AGC
DATA
SW
DOWN
CONVERTER
PREAMBLE
DET
420 KBPS
SAWDS
COHERENT
AGC
BIT SYNC
T/R SW
DATA DET
FRED
SYNTH
CONTROL
FUNCTIONS
PA
PREAMBLE
GENERATOR
UPCONVERTER
MODULATOR
ENCODER

2 of 3

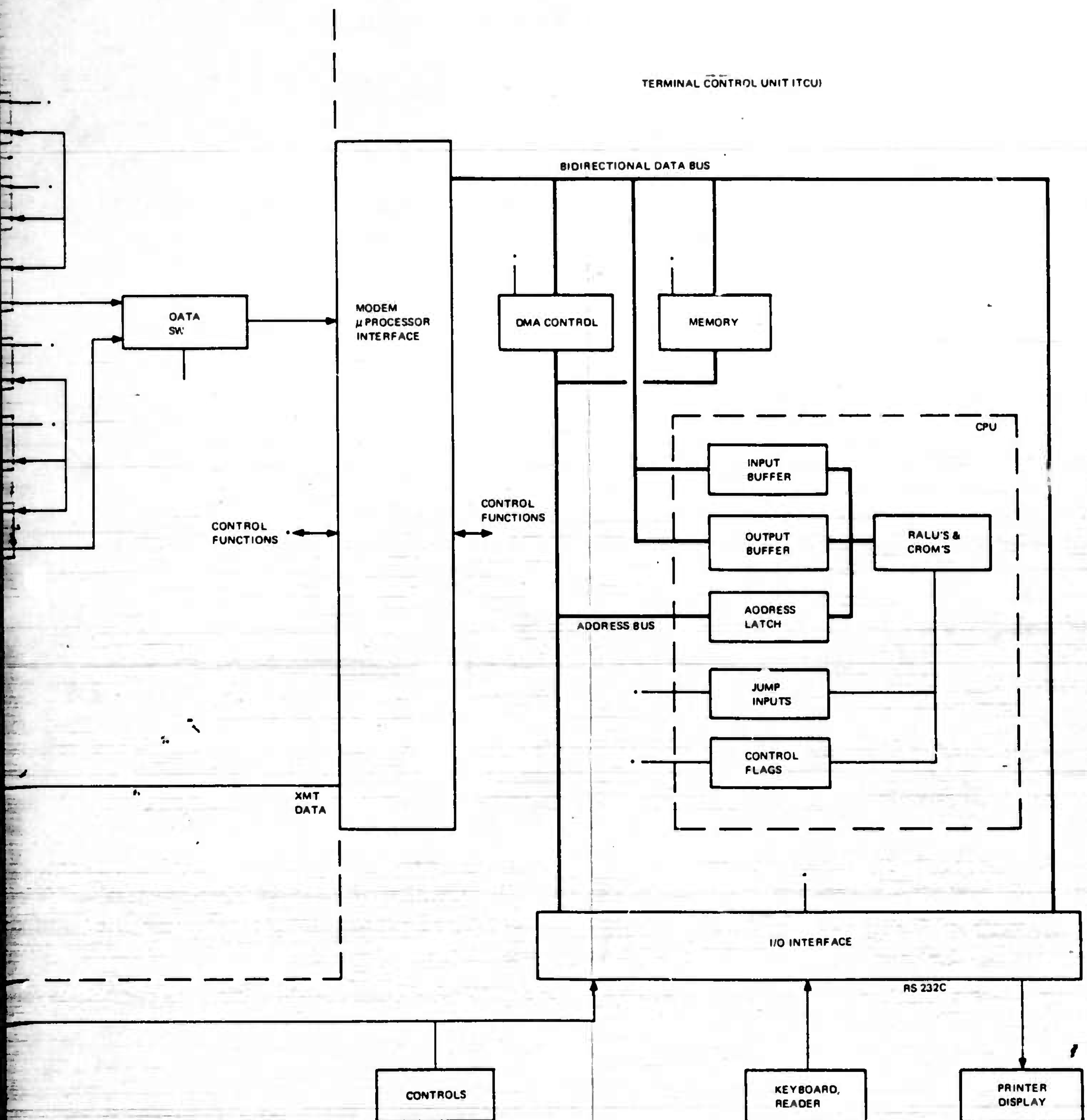


Figure 8.7-1. Terminal Composite Diagram.

2 of 3

Sense lights could include carrier sense indicator, transmitter indicator, receiver indicator, and other miscellaneous indicators considered of value. Loop tests should be available for the user to test his entire local system for both transmission and reception and he should also be able to test links to the repeater and/or station in similar manners.

Network protocol and channel access control programs should reside in PROM's which can be easily replaced. Under no conditions should RAM memory be used for control programs due to its vulnerability to power failure.

The TCU must be able to recognize Network Performance commands similar to those in the ARPANET. In this respect, the TCU's must function as IMP's although there will be a limit to the cumulative data they can provide due to lack of memory capacity and loss of memory due to power loss.

8.8 PROTOTYPE STATION CONFIGURATION

The station must interface with repeaters and thus will electrically have all the capability of a repeater. In addition it will have the crypto and additional computing capability.

8.8.1 Capability Summary

The station is the hub of radio access to the ARPANET and must handle the most traffic. Optional multiple detectors would probably be required first at a station as traffic density increases.

8.8.2 Composite Diagram

See figure 8.8-1 for a station composite diagram.

8.8.3 Power Sources and Distribution

The power considerations are essentially the same as for the repeater equipment. Long cable runs between the modem and the equipment mounted at the antenna might require additional line amplifiers. The power source for the equipment will still be +24 volts dc but can be obtained from an ac source at the station.

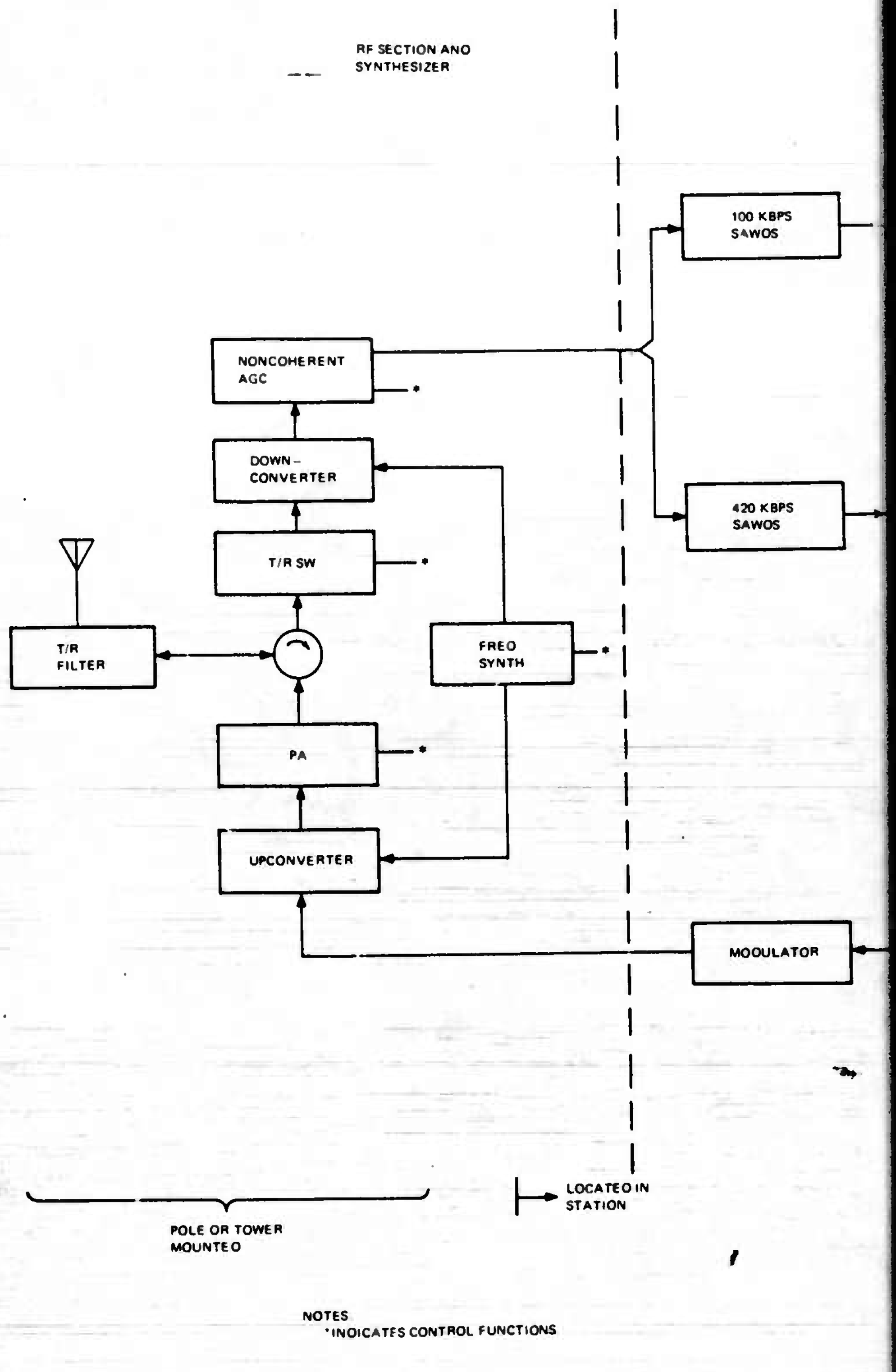
8.8.4 Physical Description

The station unit offers several possible configurations. Assuming a transportable one unit type configuration, the unit may be the same as the repeater unit measuring 7.50" wide x 7.65" deep x 23.4" high. The unit may be configured as two units; the rf/antenna section, and a card cage section similar to the repeater option. The two unit system offers the advantages of improved antenna performance with only a slight weight increase. For maintenance and testing, the two section approach is most desirable. The rf section can be placed on a mast and the card cage section close to the host processor. Long lengths of line carrying digital information are thus avoided.

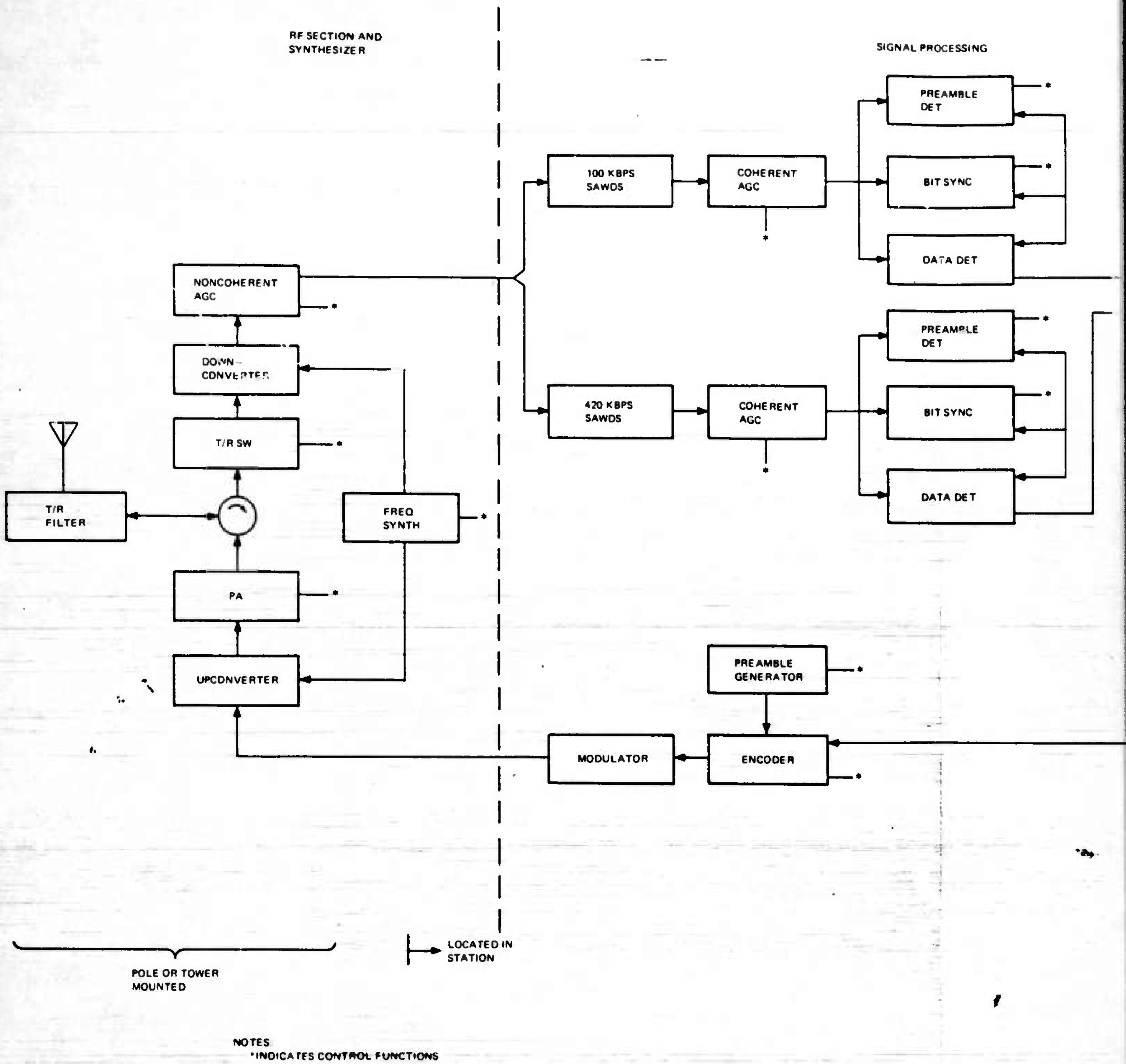
8.8.5 Maintenance and Testing

The station system is the logical point for radio network management and control. The equipment must have all the test capabilities of a terminal plus all the software and hardware to request and receive maintenance and traffic data reported by repeaters.

(The radio network maintenance and test philosophy will be supplied later with a plan for implementing that philosophy.)


RF SECTION AND
SYNTHESIZER
100 KBPS
SAWOS
NONCOHERENT
AGC
DOWN-
CONVERTER
420 KBPS
SAWOS
T/R SW
T/R
FILTER
FREQ
SYNTH
PA
UPCONVERTER
MODULATOR
POLE OR TOWER
MOUNTED
LOCATED IN
STATION
NOTES
*INDICATES CONTROL FUNCTIONS

1of 3



RF SECTION AND SYNTHESIZER
SIGNAL PROCESSING
PREAMBLE DET
100 KBPS SAWDS
COHERENT AGC
BIT SYNC
DATA DET
NONCOHERENT AGC
PREAMBLE DET
DOWN-CONVERTER
420 KBPS SAWDS
COHERENT AGC
BIT SYNC
T/R SW
T/R FILTER
FREQ SYNTH
DATA DET
PA
PREAMBLE GENERATOR
UPCONVERTER
MODULATOR
ENCODER
LOCATED IN STATION
POLE OR TOWER MOUNTED
NOTES
*INDICATES CONTROL FUNCTIONS

2 of 3

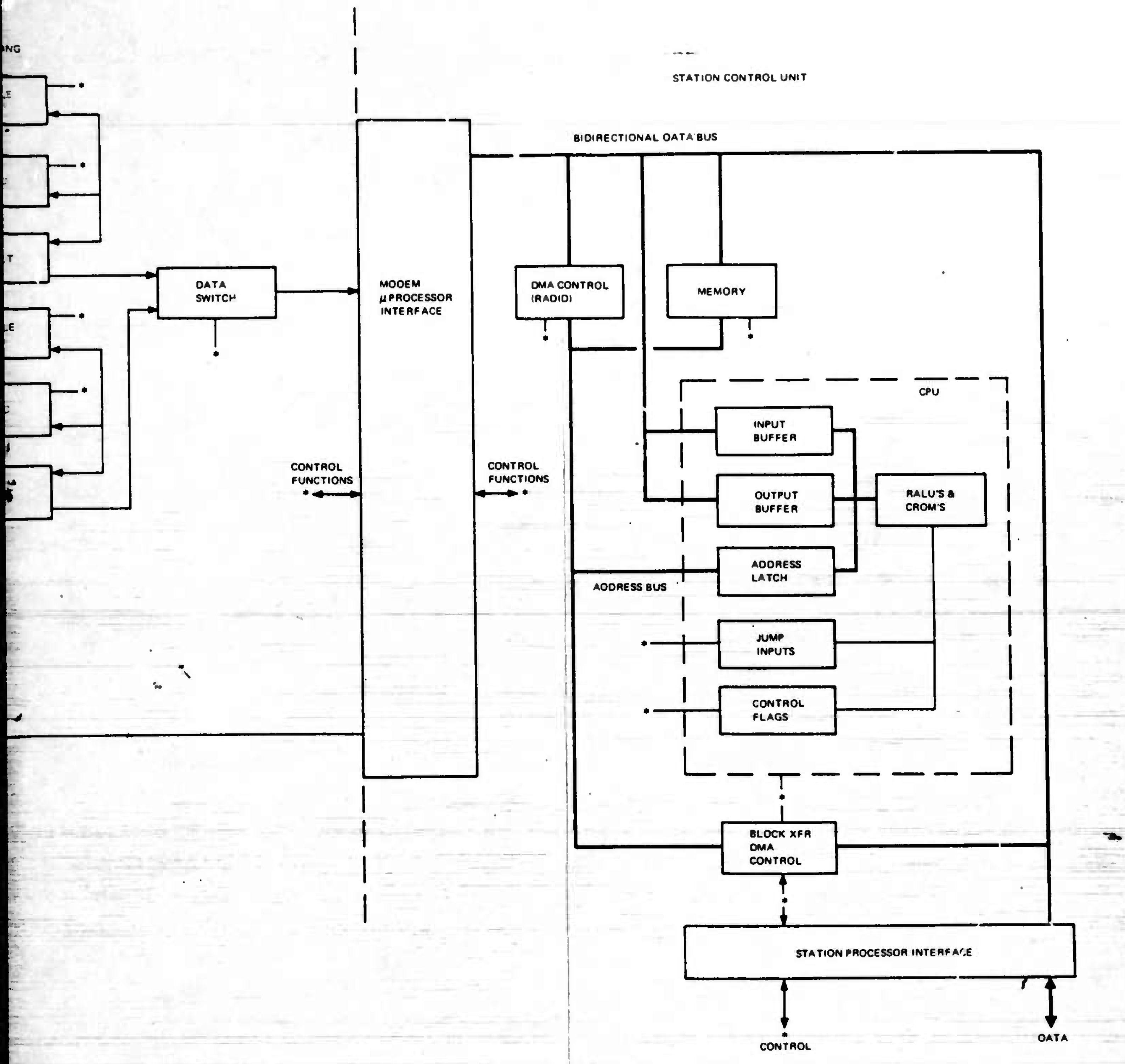


Figure 8.8-1. Station Composite Diagram.

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